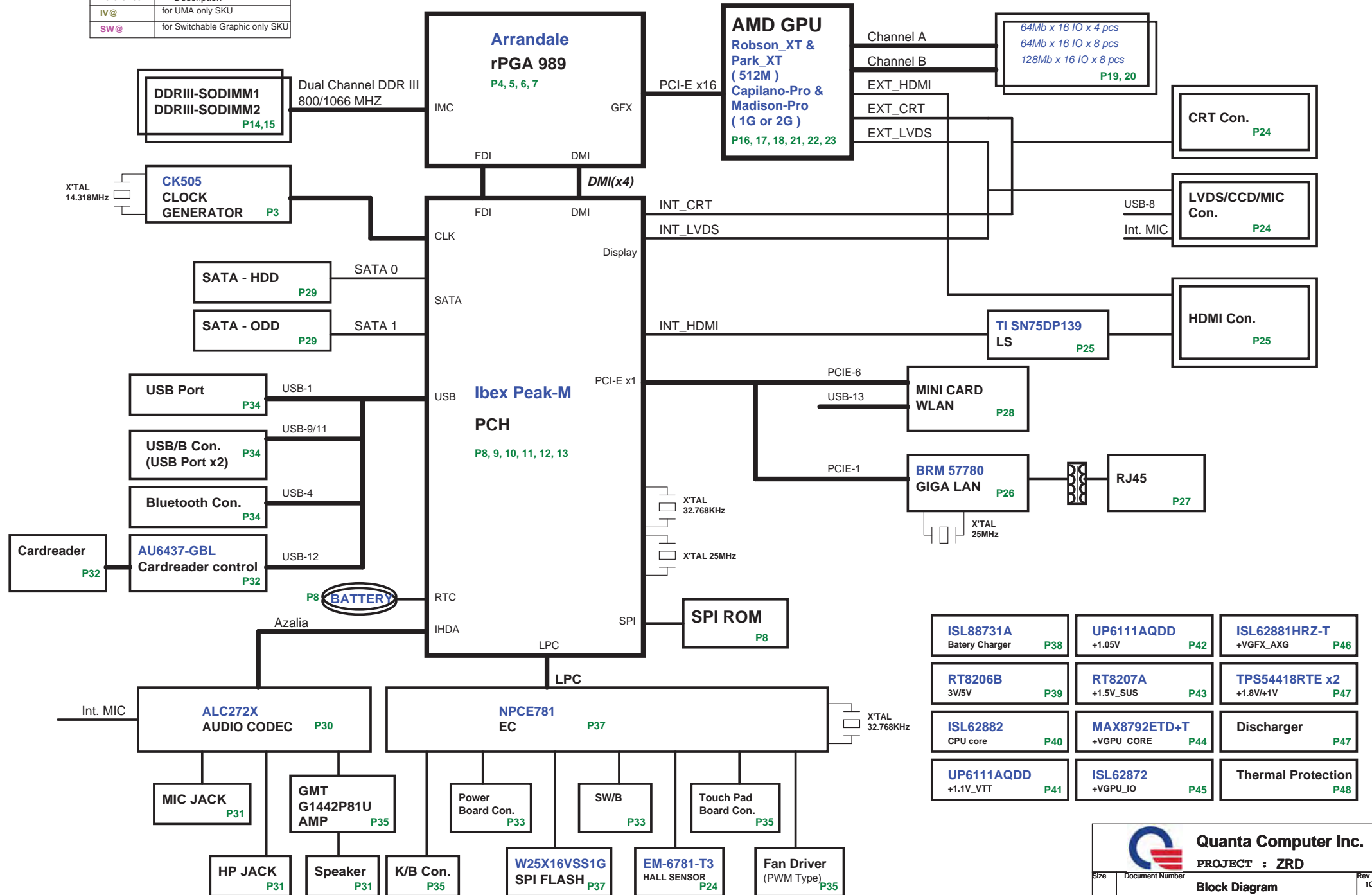


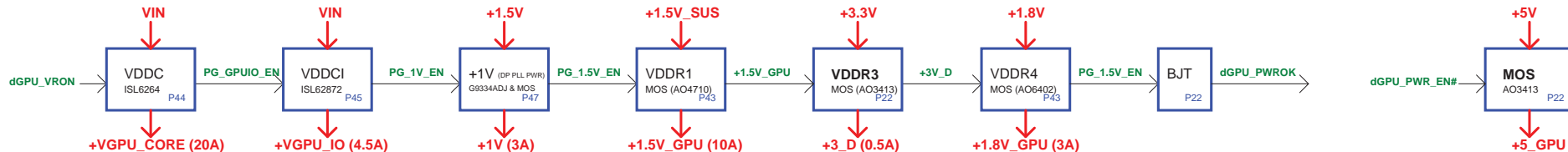
HM55_CP (ZRD) SYSTEM BLOCK DIAGRAM

BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU



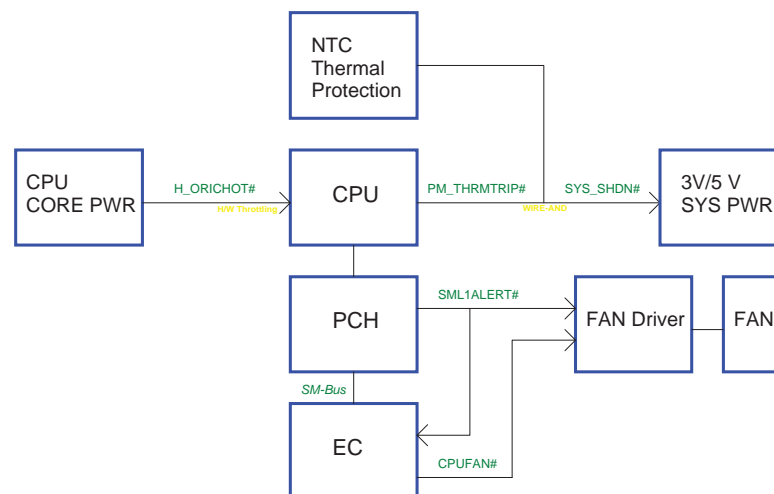
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

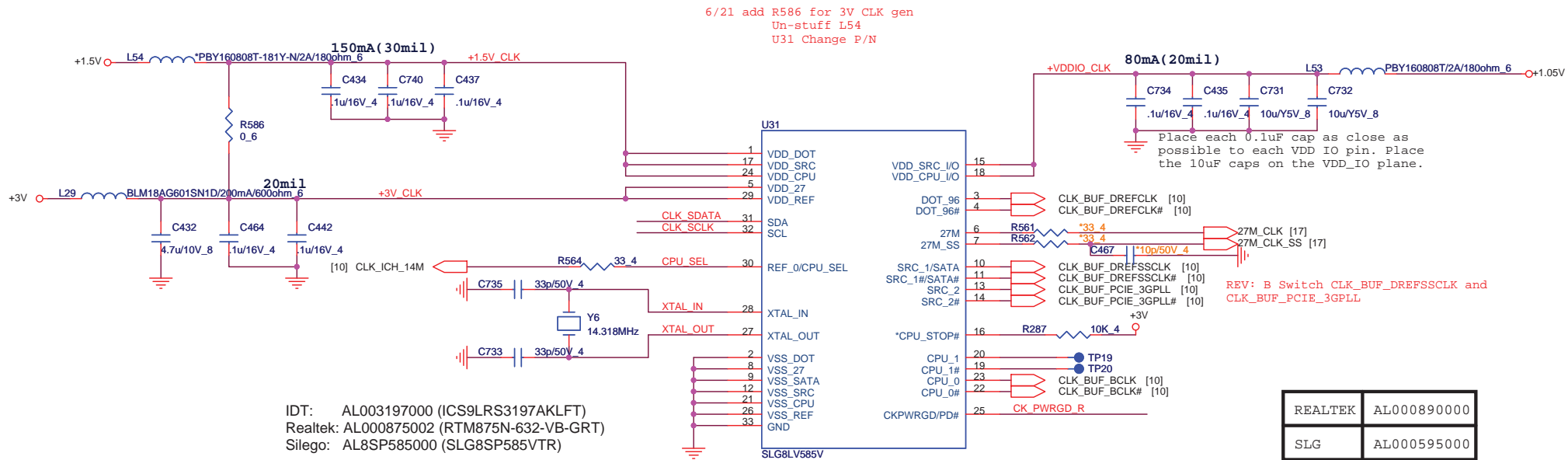


Power States

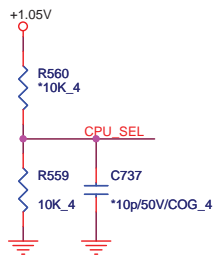
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



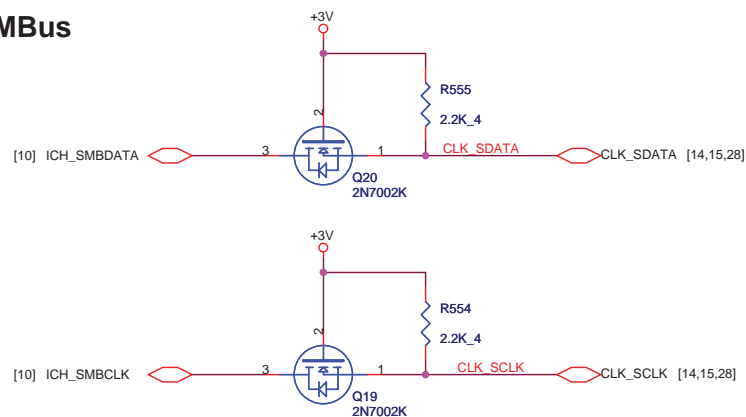


CPU_CLK select

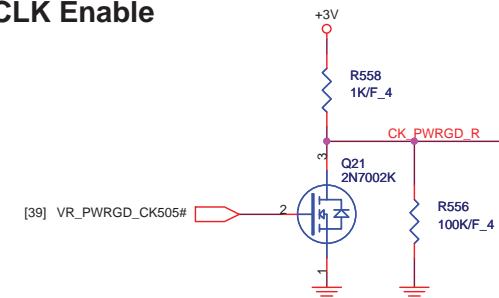


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



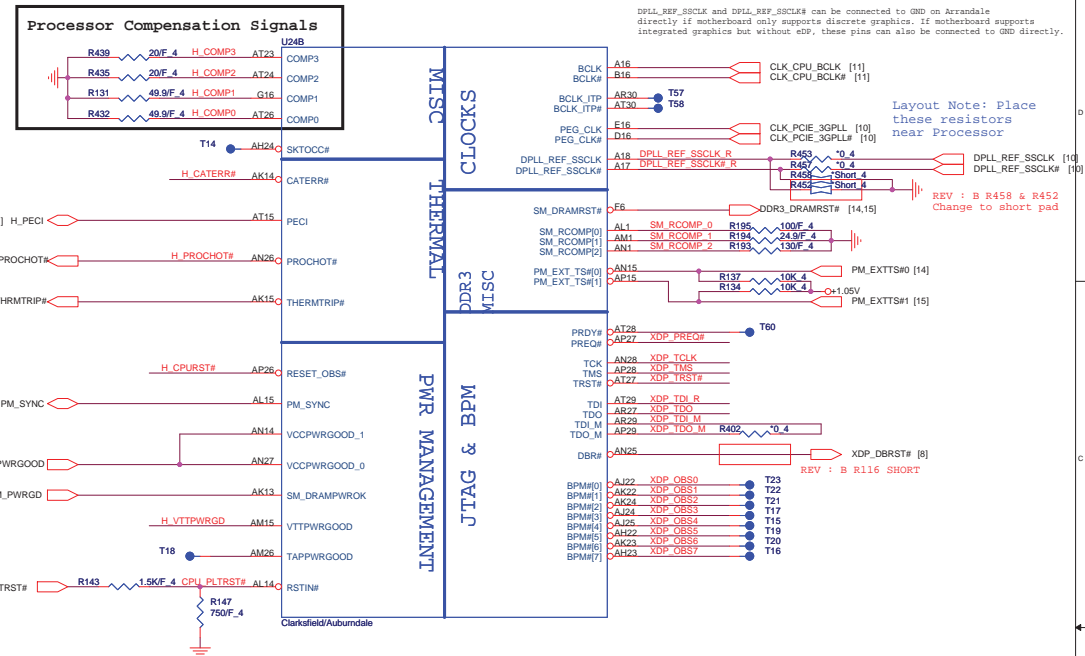
CLK Enable



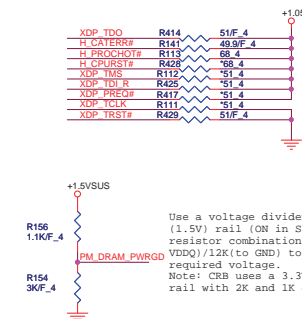
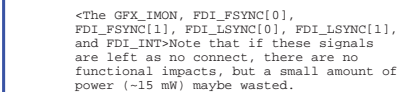
Quanta Computer Inc.

PROJECT : ZRD

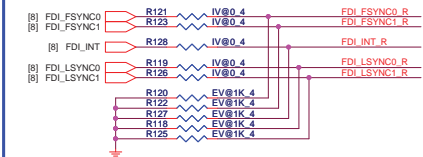
Size	Document Number	Rev
	Clock Generator	1C
Date:	Wednesday, July 21, 2010	Sheet 3 of 46



LTS	DGG^9000005
SUY	DGG^9000016
FOX	DGG^9000023



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.



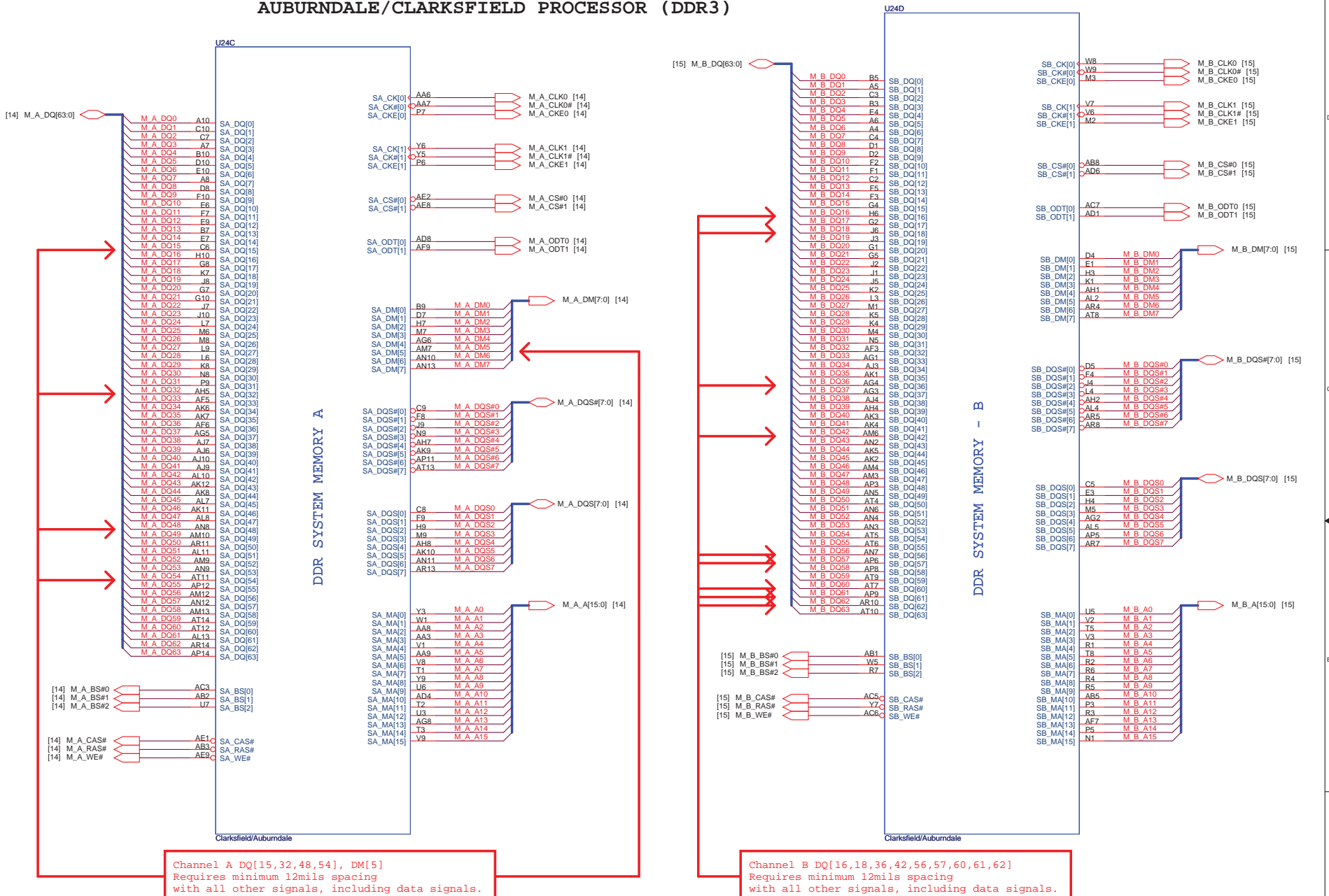
<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.



PROJECT : ZRD

Size	Document Number	Rev
	AUBURND 1/4	10
Date:	Wednesday, July 21, 2010	Sheet 4 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

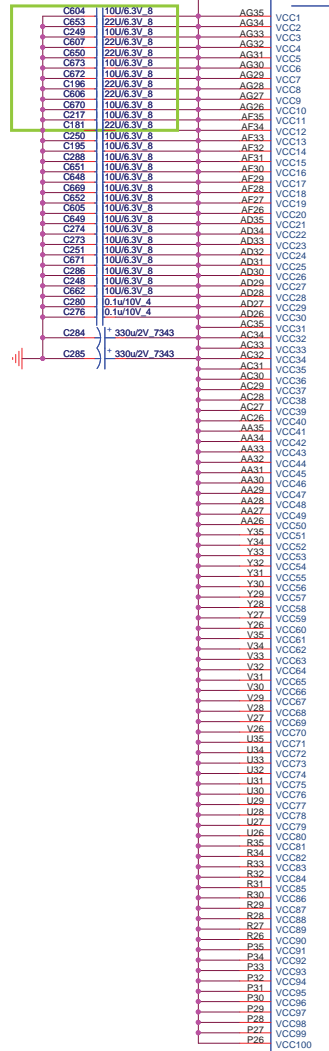


CPU Core Power

U24F

ARD:48A
CFD:52A

+VCC_CORE



Clarksfield/Auburndale

AUBURNDAL/CLARKSFIELD PROCESSOR (POWER)

VTT Rail Values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

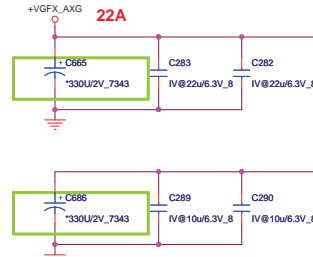
18A

+1.05V

AUBURNDAL/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

+VGFX_AGX

22A



U24G

GRAPHICS

POWER

SENSE LINES

DDR3 - 1.5V RAILS

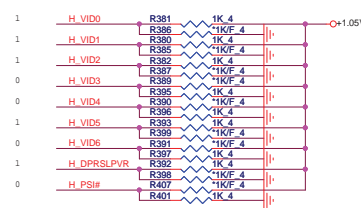
1.1V

1.8V

FBI

PG & DWI

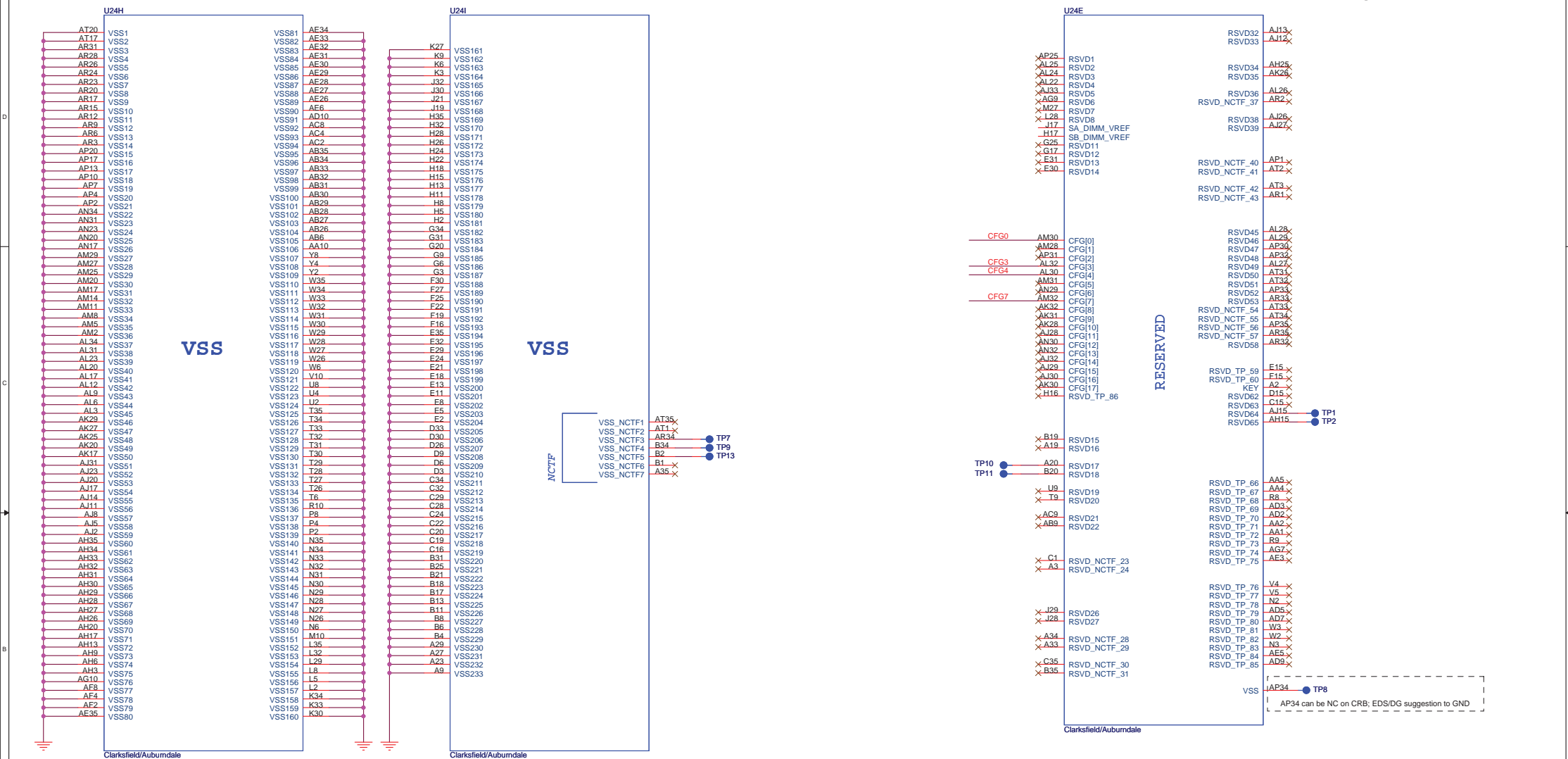
Clarksfield/Auburndale

NOTE:
For Validating DM9 VR R6451 should be STUFF
and R2N1 NO_STUFFHFM_VID : Max 1.4V
LFM_VID : Min 0.65VQuanta Computer Inc.
PROJECT : ZRDSize Document Number
AUBURNDAL 3/4 (PWR)
Date: Wednesday, July 21, 2010 Sheet 6 of 46

Rev 1C

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

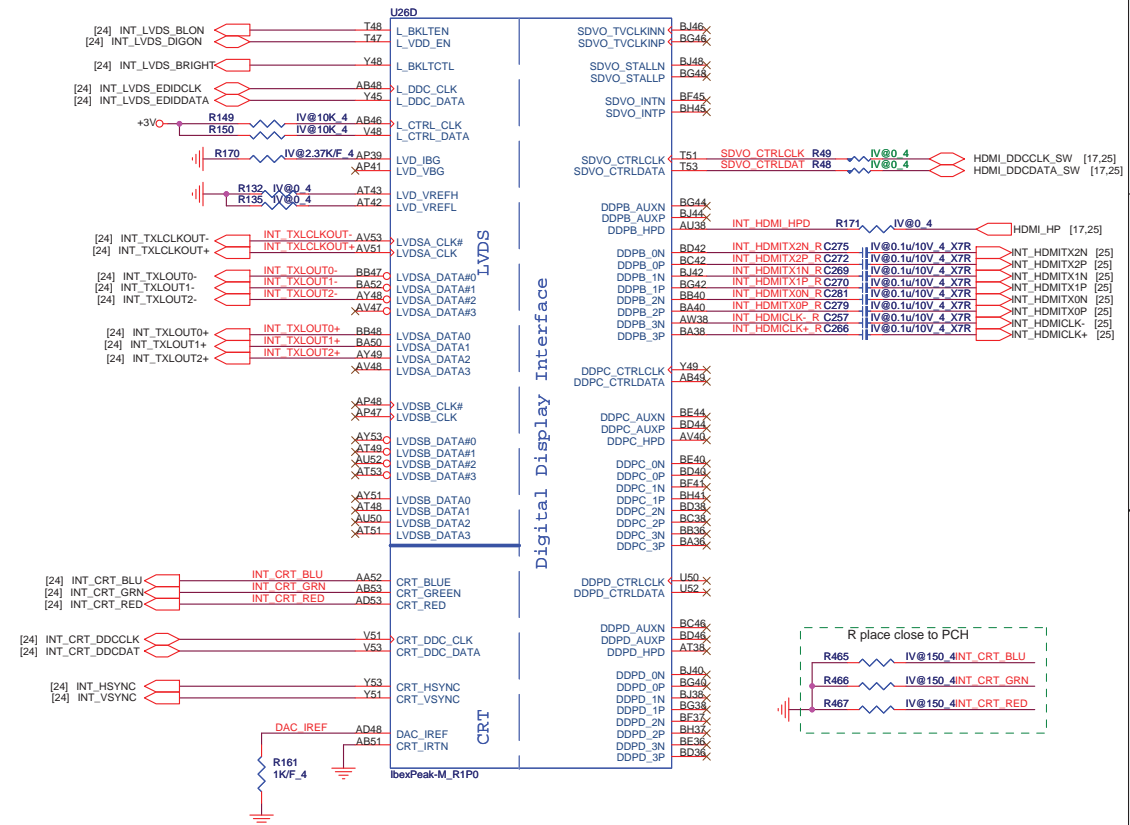


Processor Strapping

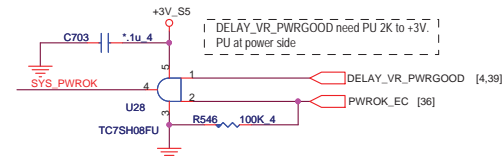
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.				

AC-coupling CAP place close to PCH

IBEX PEAK-M (LVDS, DDI)



System PWR_OK



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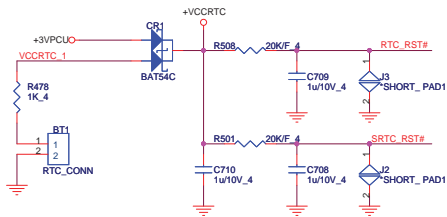
PROJECT : ZRD

Size	Document Number IBEX PEAK-M 1/6
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Date: Wednesday, July 21, 2010

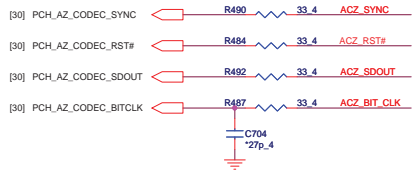
Sheet 8 of 46

RTC Circuitry

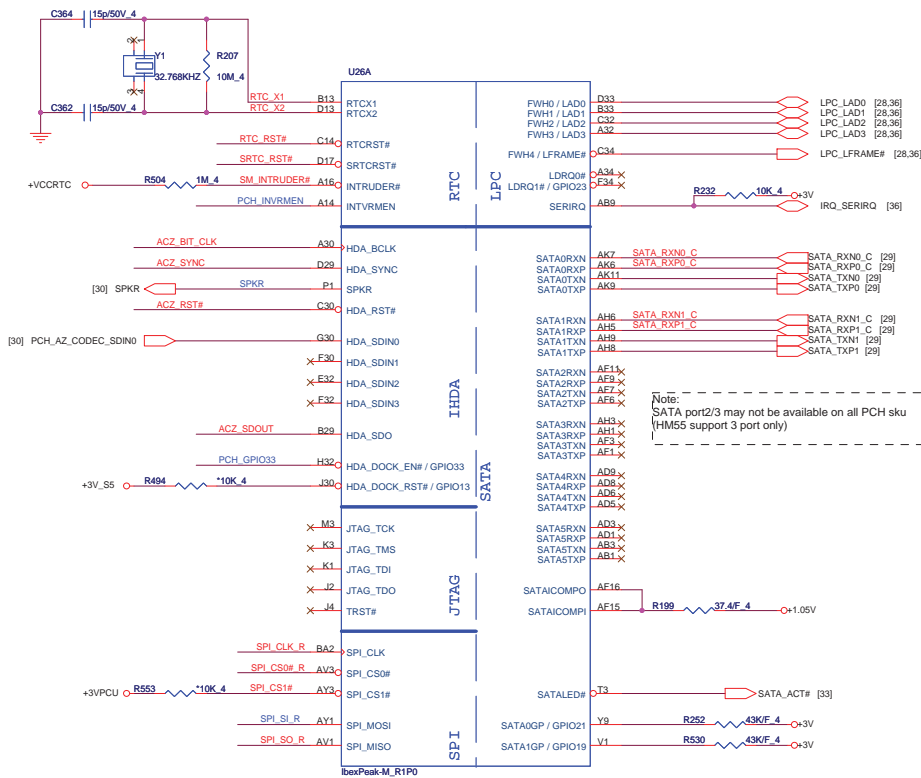
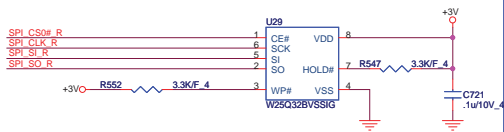


HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V

HDA Bus



PCH SPI

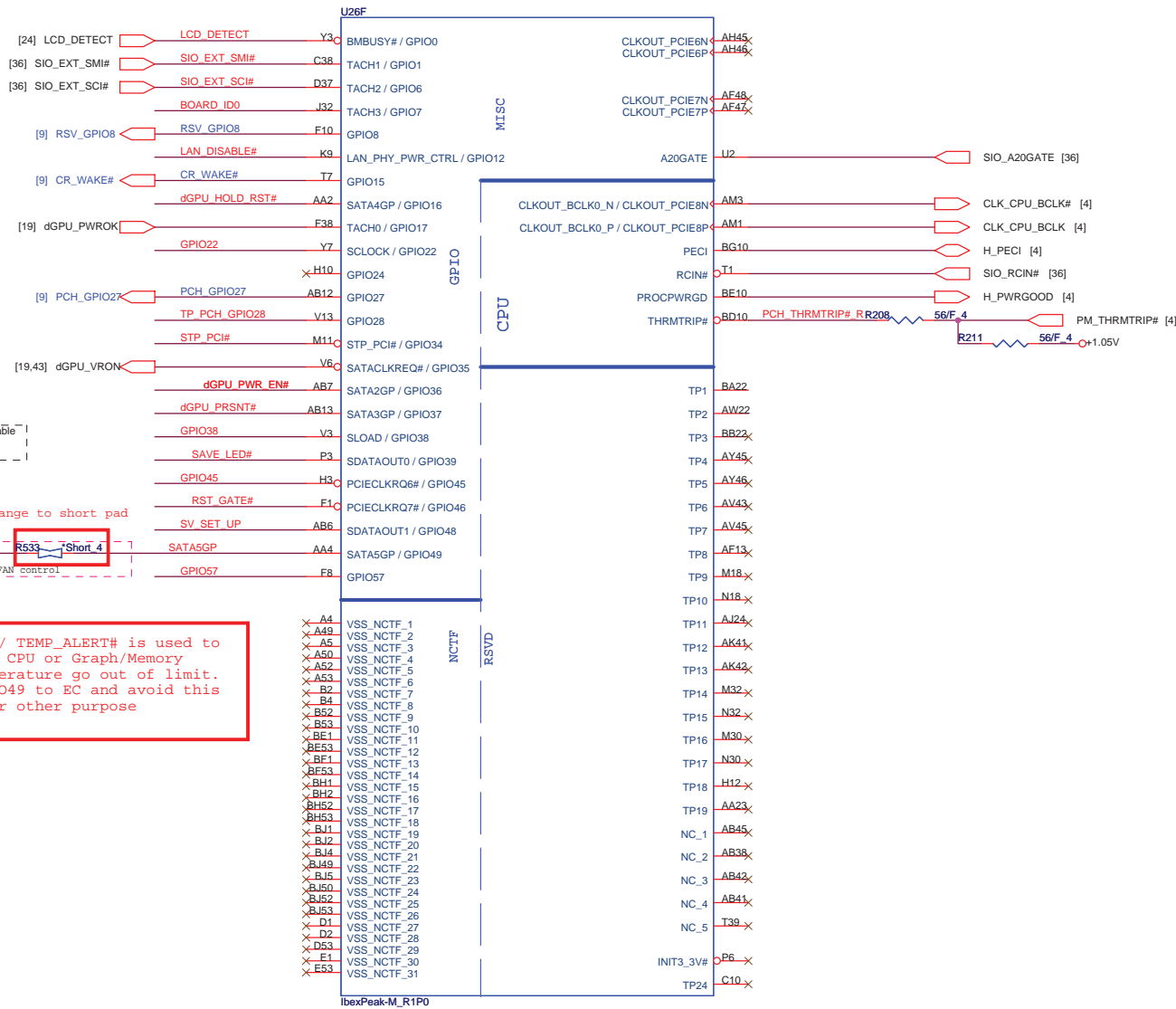


PCH Strap Pin Configuration Table-1

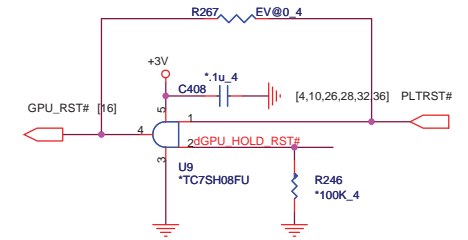
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R511 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disabled	+3V R551 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R538 1K 4 SPI_SO_R
HDA_DOCK_EN# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J1 1 2 *SHORT_PAD1
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCL_GNT0# R158 1K 4 [10] PCL_GNT1# R152 1K 4 [10] PCL_GNT1# R150 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	[10] PWM_SELECT# R182 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCL_GNT3# R462 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE R213 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	[10] NV_CLE R216 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] RSV_GPIO8 R215 10K 4 +3V_S5 R214 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] CR_WAKE# R256 1K 4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	[11] PCH_GPIO27 R231 10K 4



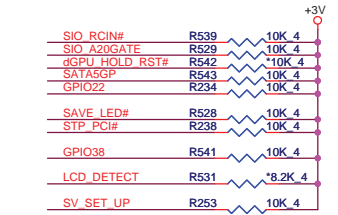
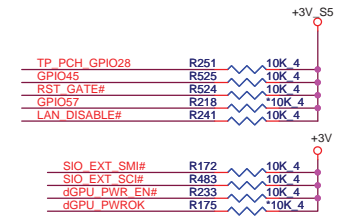
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



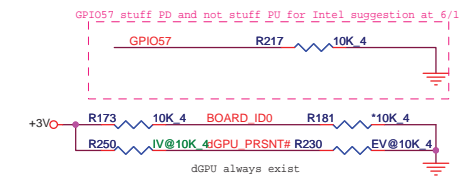
GPU RST#



GPIO Pull-up/Pull-down



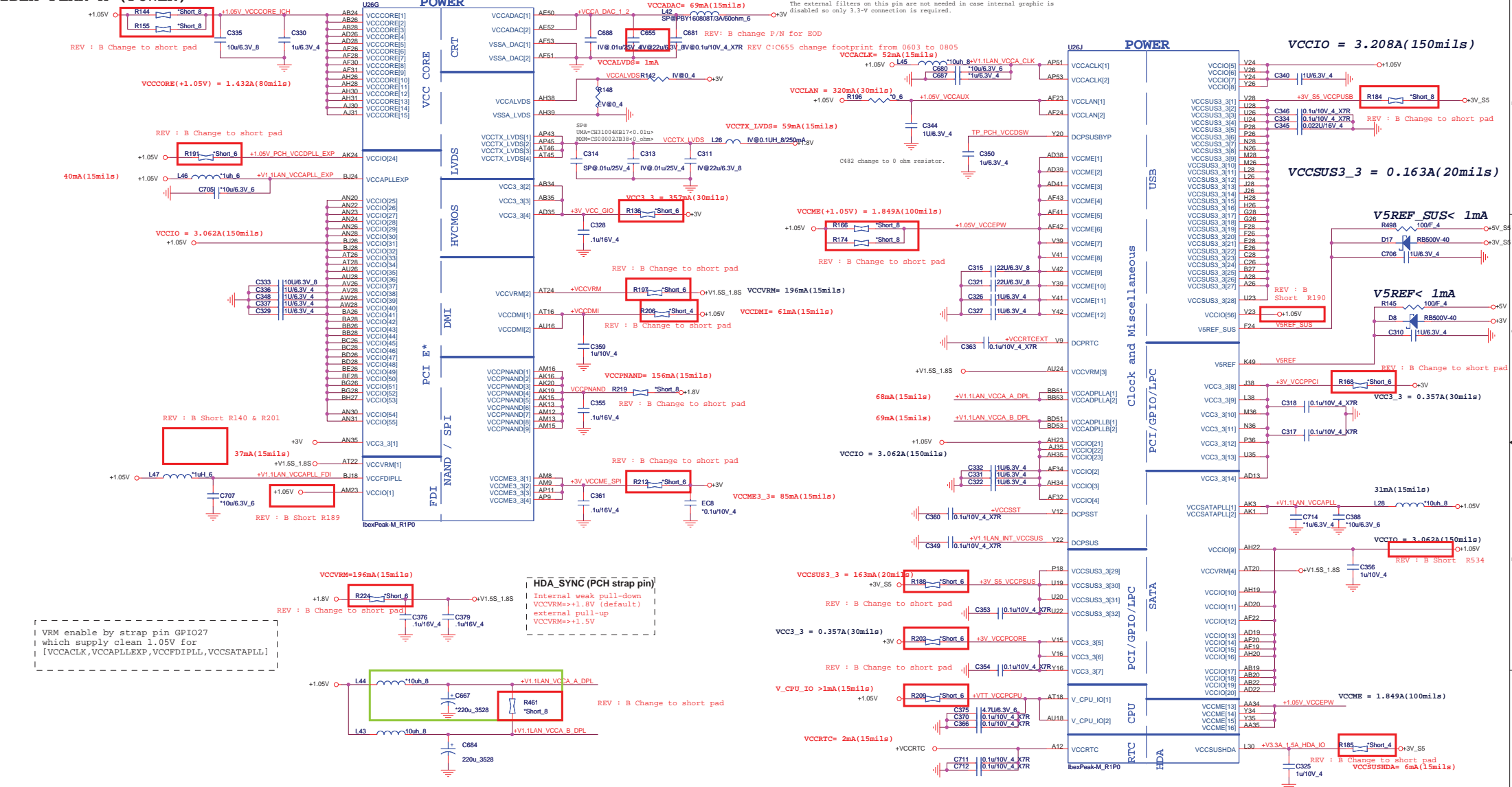
SV_SET_UP 1-X High = Strong (Default)



BOARD_ID0 High = 15" Low = 14"



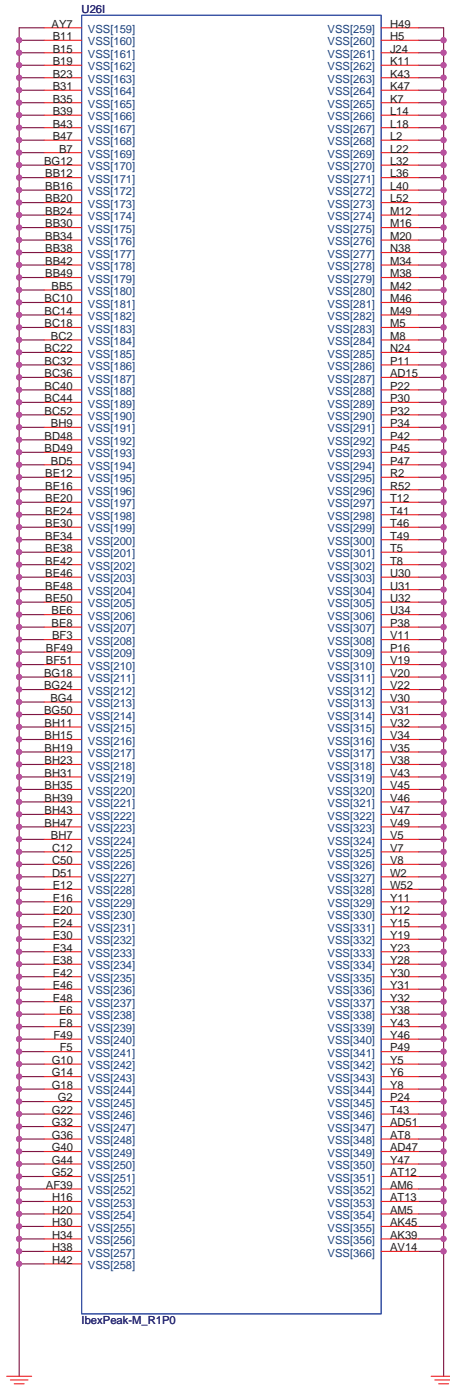
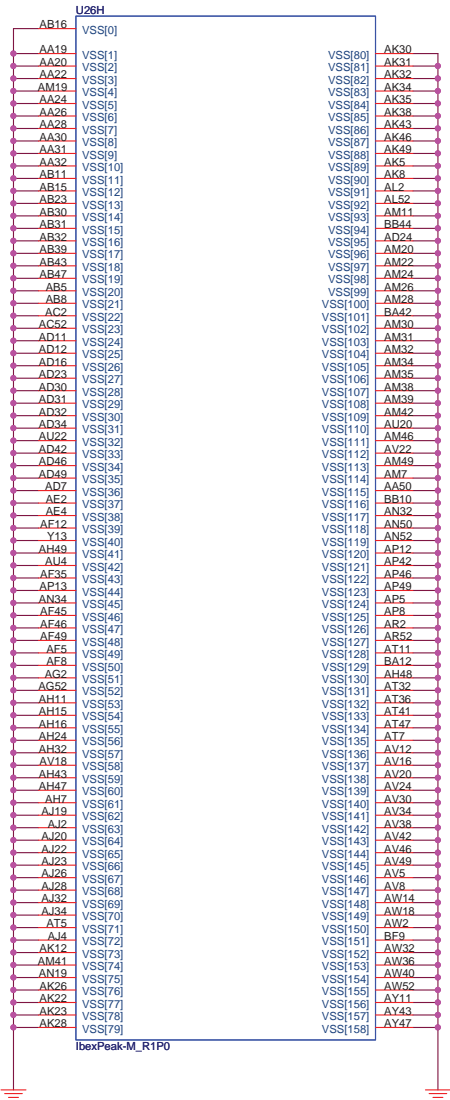
IBEX PEAK-M (POWER)



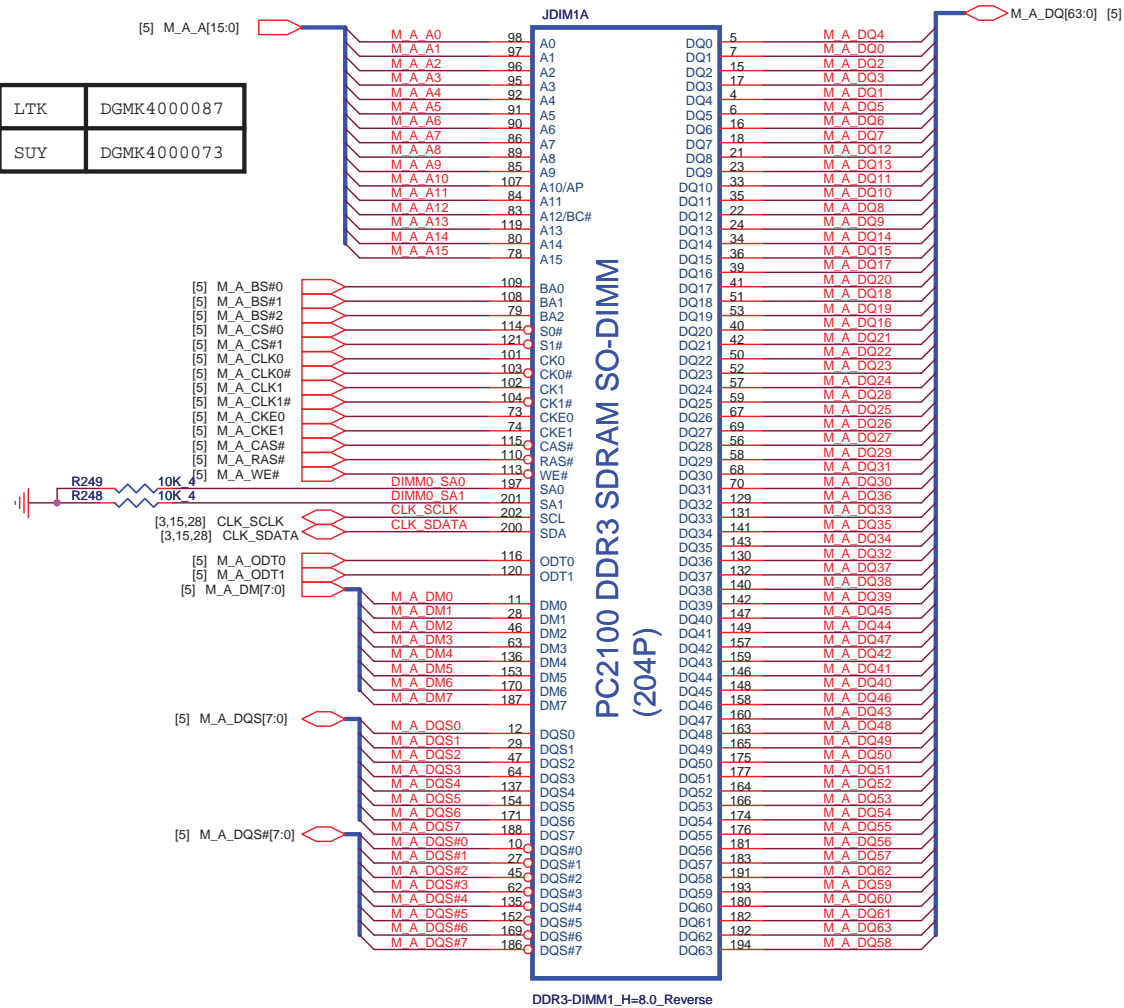
PROJECT : ZRI

Size	Document Number	Rev
	IBEX PEAK-M 5/6	1C
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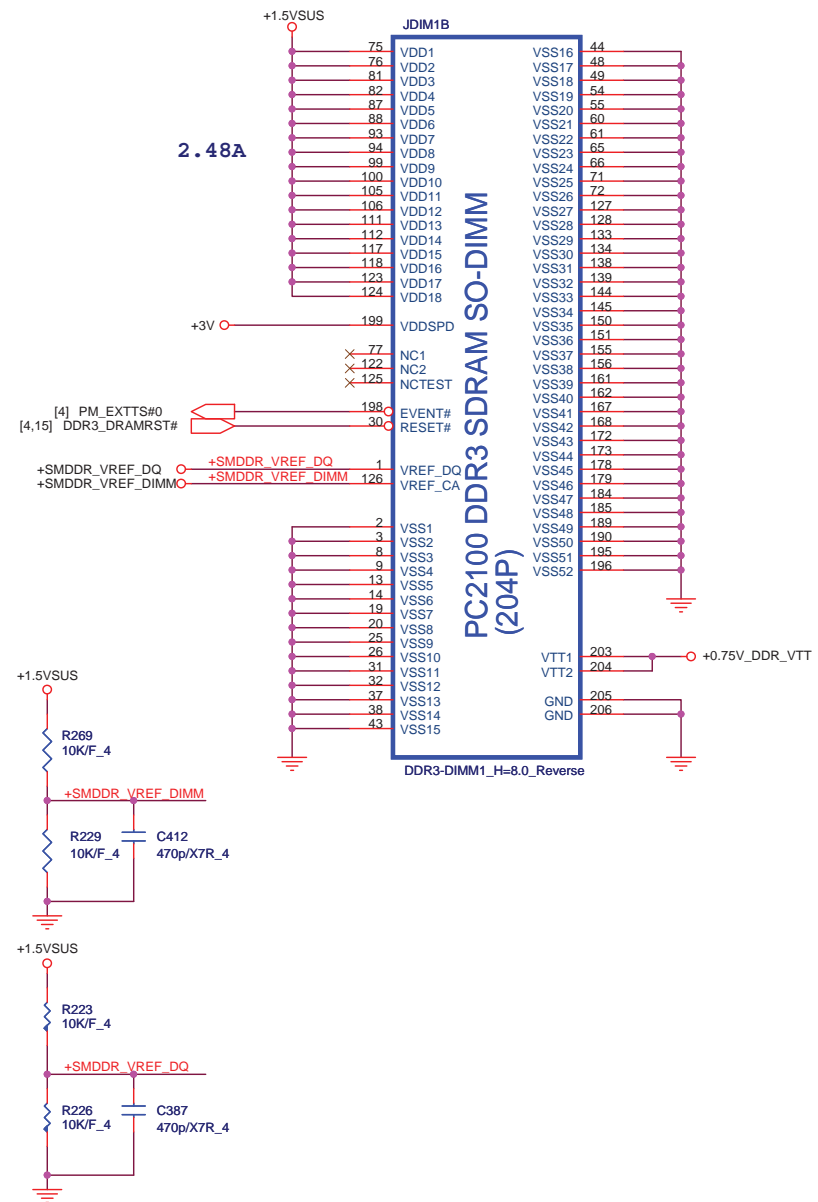
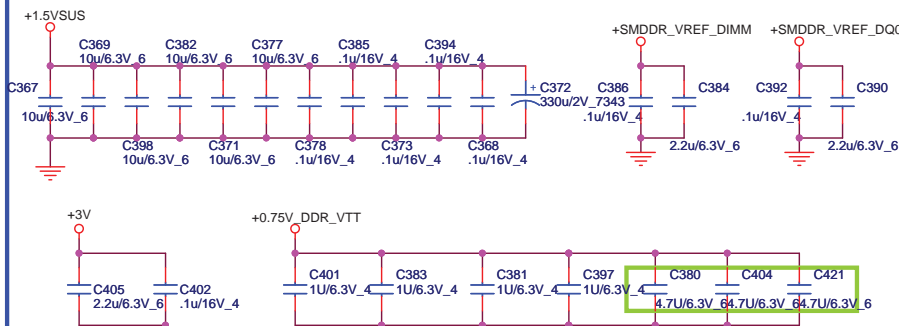
IBEX PEAK-M (GND)



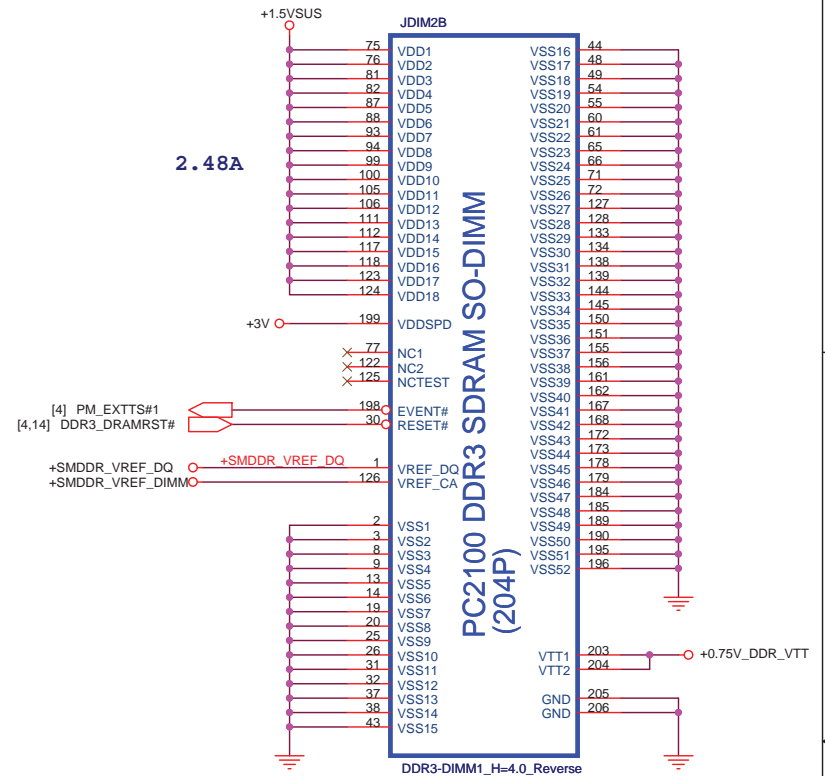
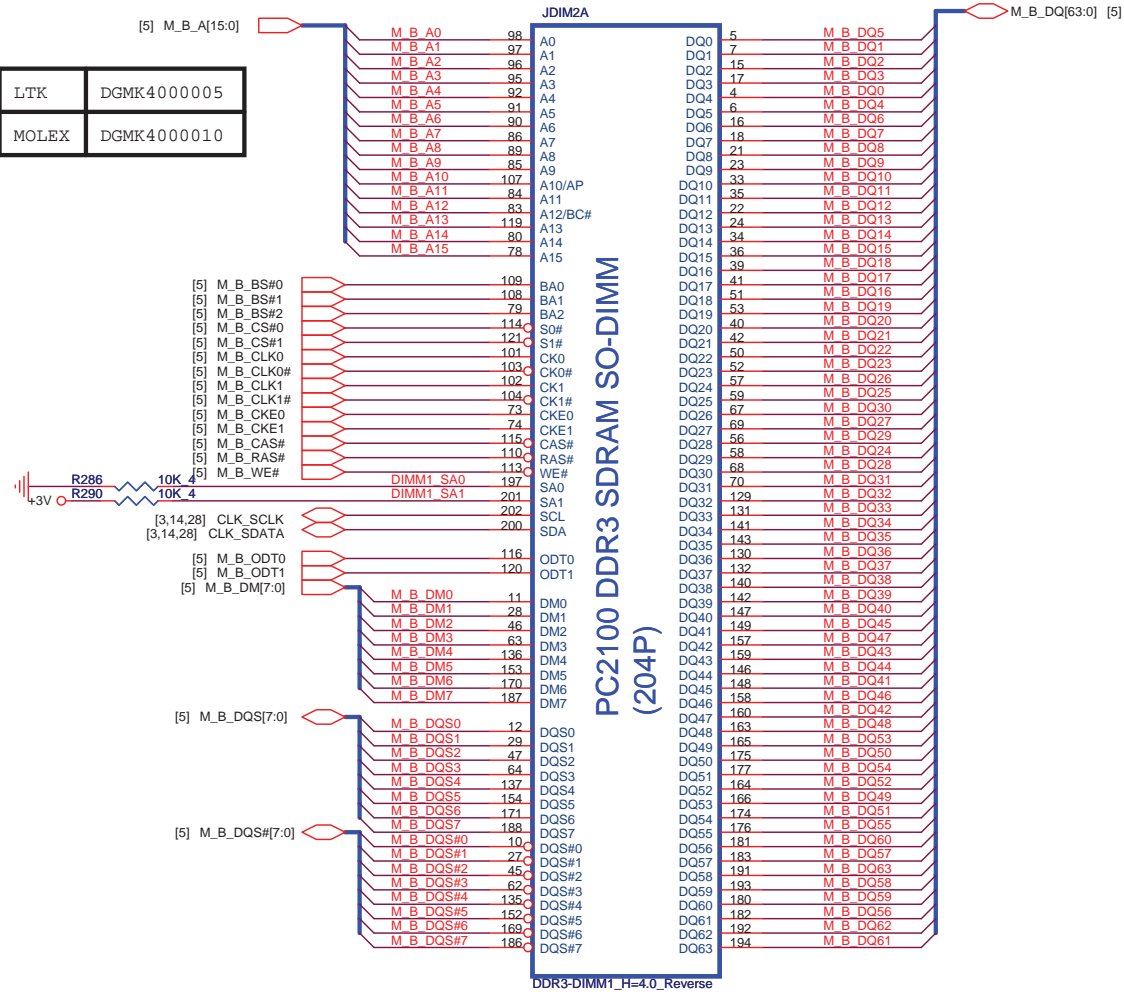
LTK	DGMK4000087
SUY	DGMK4000073



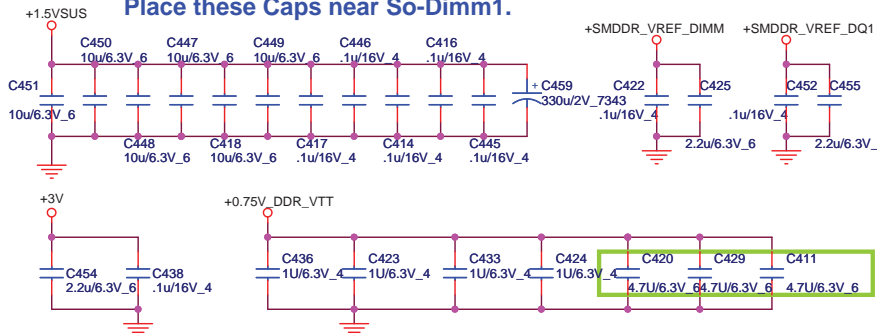
Place these Caps near So-Dimm0.



LTK	DGMK4000005
MOLEX	DGMK4000010



Place these Caps near So-Dimm1.



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PROJECT : ZRD

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1C

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GPU_1(VGA)



Madison	AJ007720T02
Park	AJ077400T08



Quanta Computer Inc.
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Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1C
Date:	Wednesday, July 21, 2010	Sheet 16 of 46

GPU Power-on sequence

1.8V GPIO

NC on Park

NC on Park

Channel D N.C for Park-M2

SP@Capilano/Robson

3.3V GPIO

DAC2 will be NC on future ASIC

REV C: C188 change footprint from 0603 to 0805

DDC AUX4 NC for Park M2

LVDS

CRT

DDC AUX7 NC for Park M2

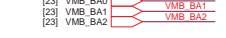


Quanta Computer Inc.

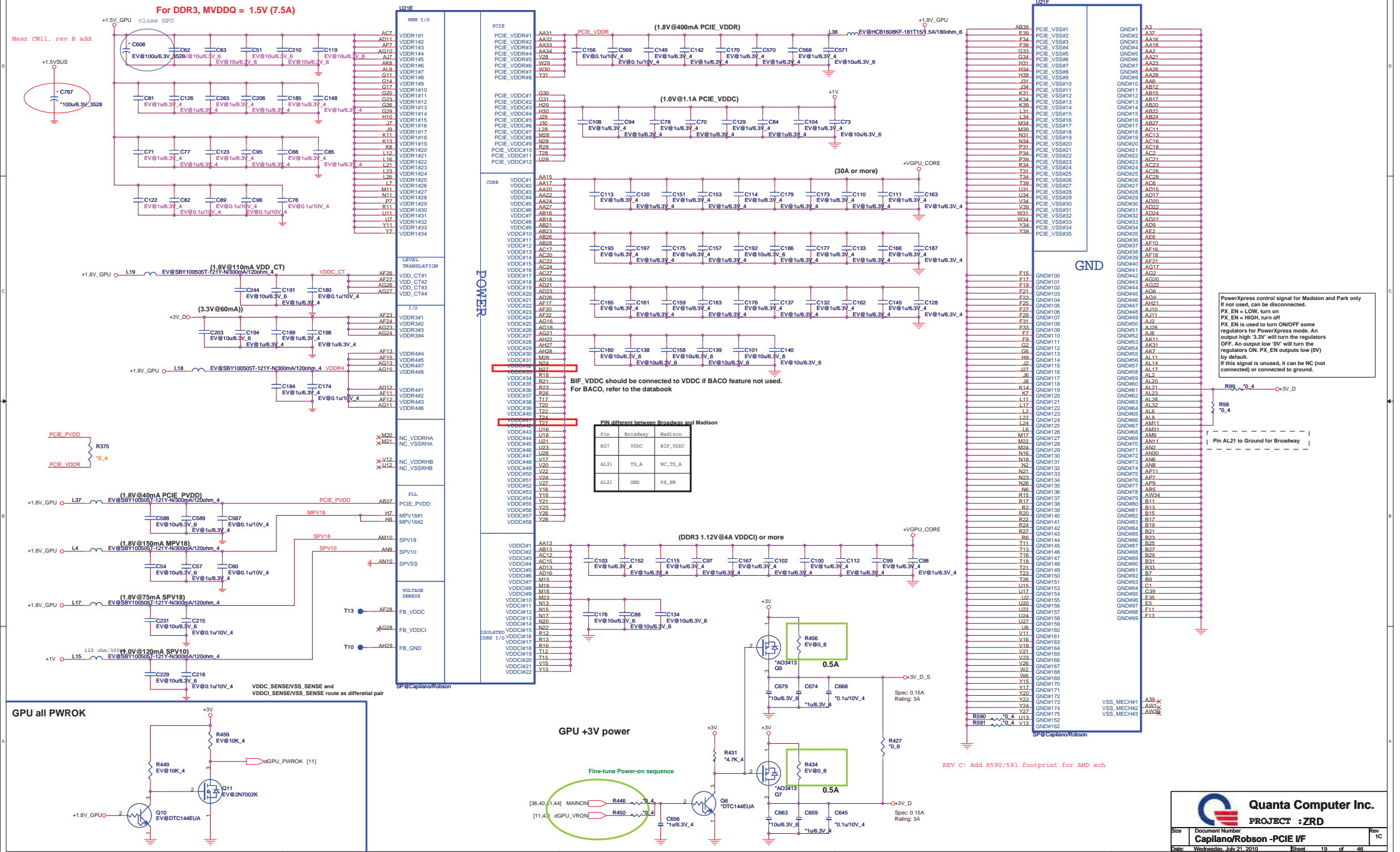
PROJECT : ZRD

Size	Document Number	Rev
	Capilano/Robson -PCIE I/F	1C
Date:	Wednesday, July 21, 2010	Sheet 17 of 46

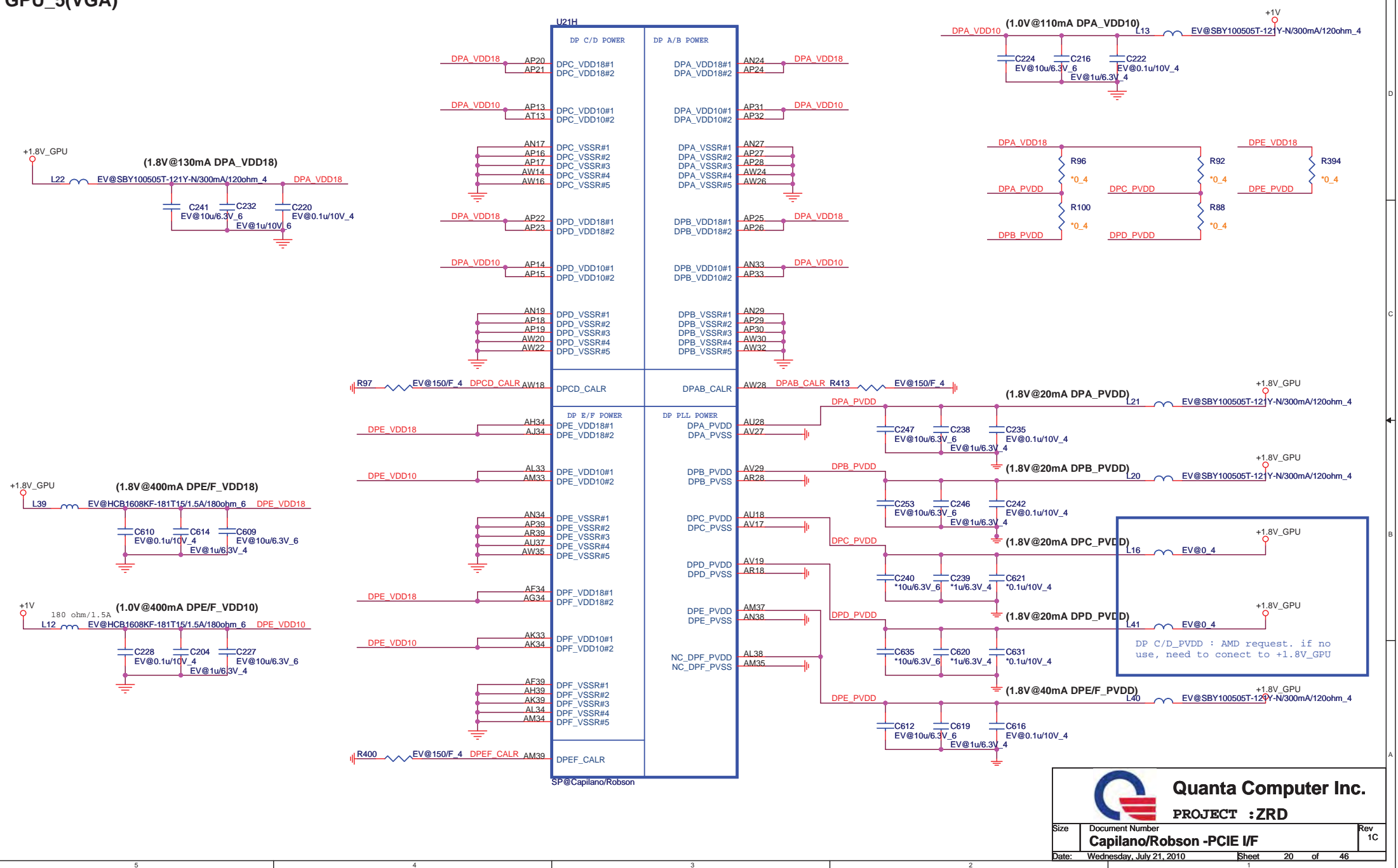
Park M2-channel B used(S3 package use Channel A)



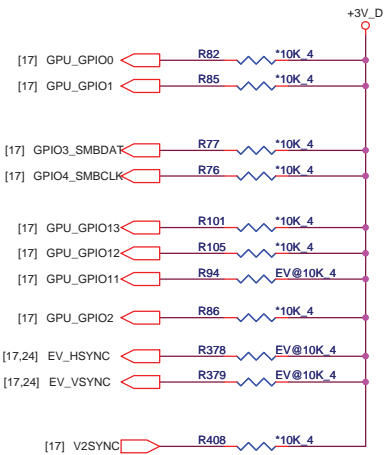
GPU_4(VGA)



GPU_5(VGA)



PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

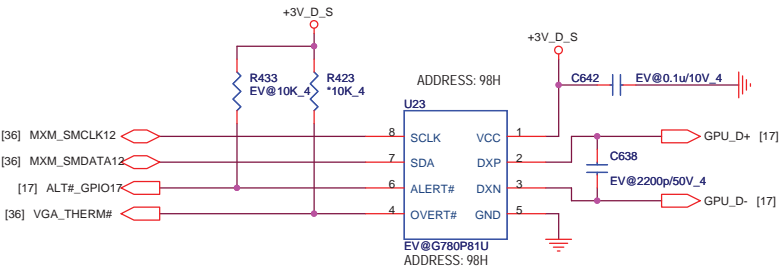
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

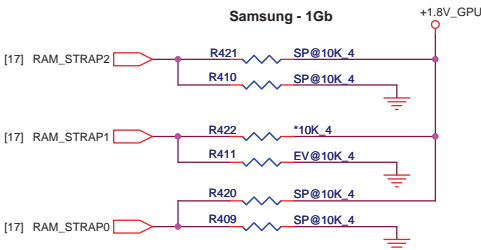
USD0.16




DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD					
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

**Quanta Computer Inc.**
PROJECT :ZRD

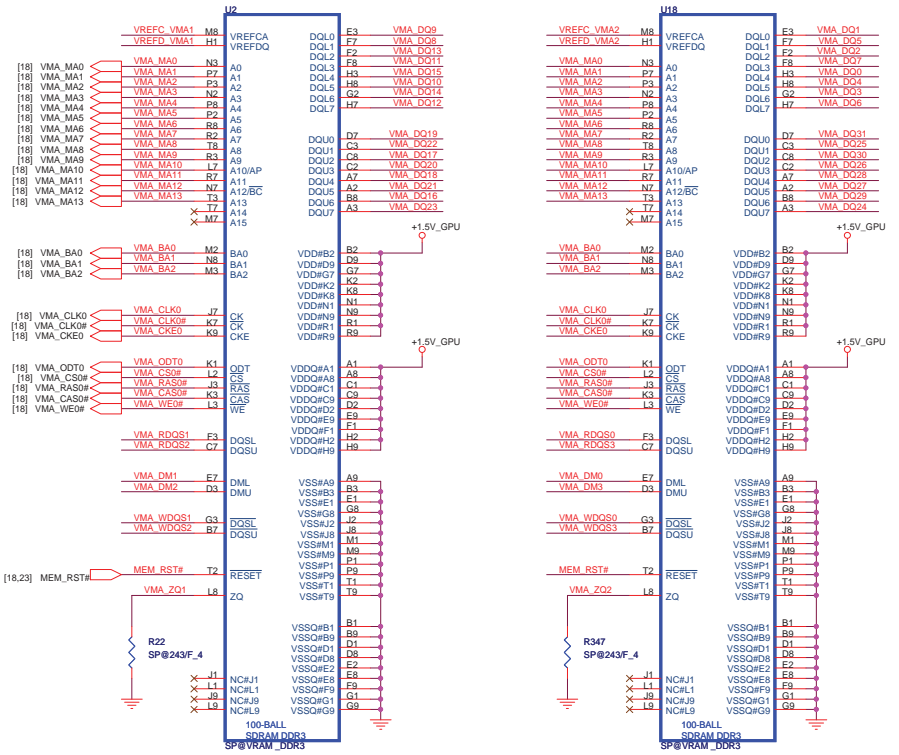
SizeDocument NumberStrip/ThermalRev1C

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CHANNEL A: 512MB DDR3 (64M*16*4pcs)

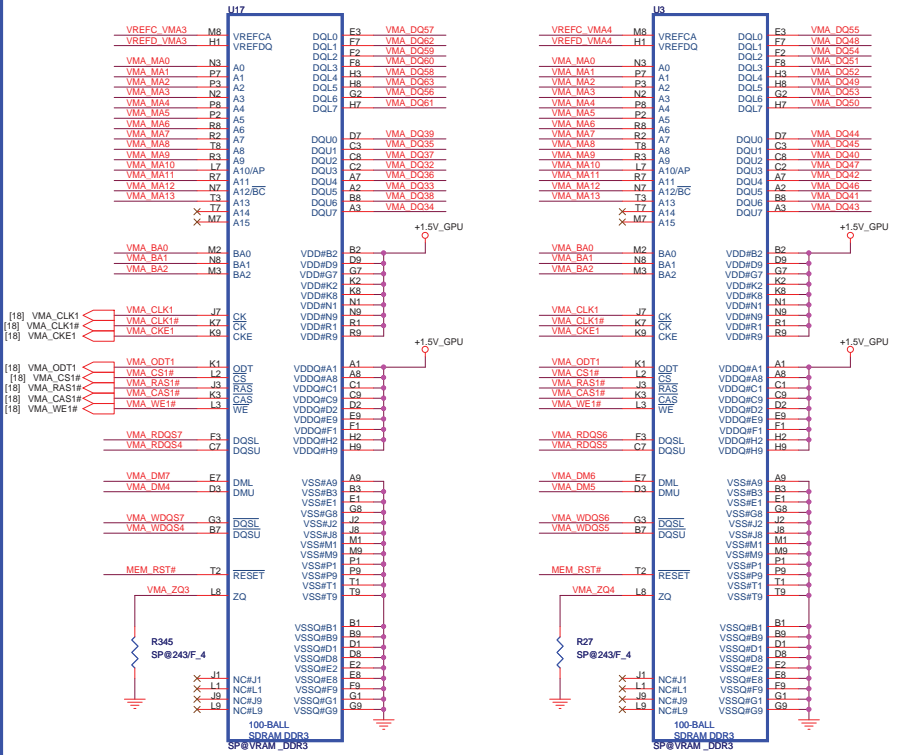
[18] VMA_DQ[63..0] VMA_DQ[63..0]
 [18] VMA_DM[7..0] VMA_DM[7..0]
 [18] VMA_RDQS[7..0] VMA_RDQS[7..0]
 [18] VMA_WDQS[7..0] VMA_WDQS[7..0]

QSA[7..0]
 QSA#[7..0]



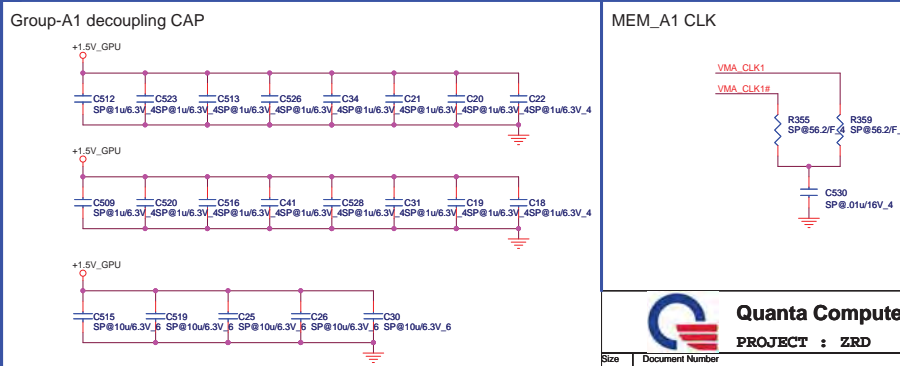
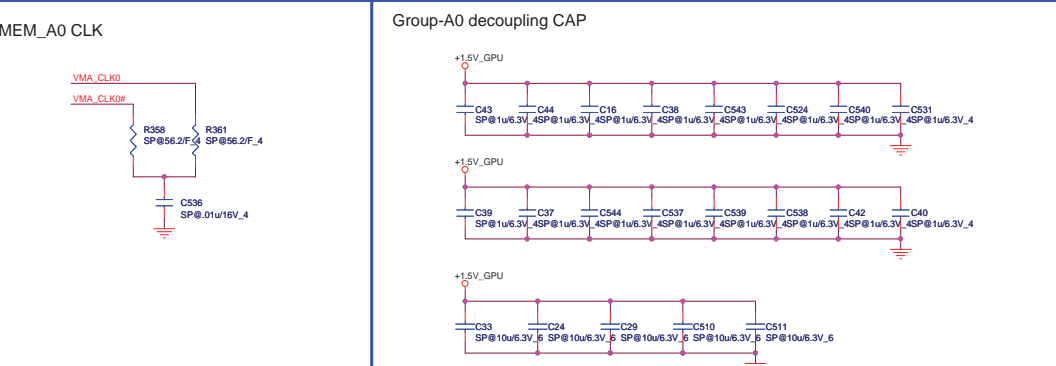
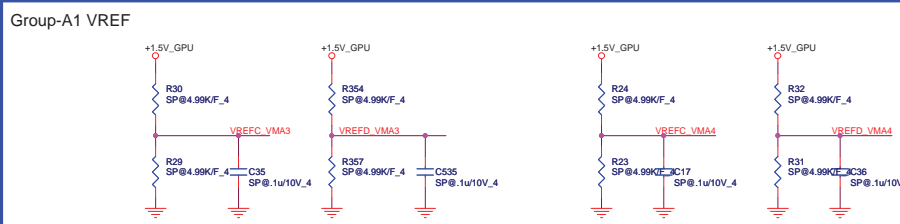
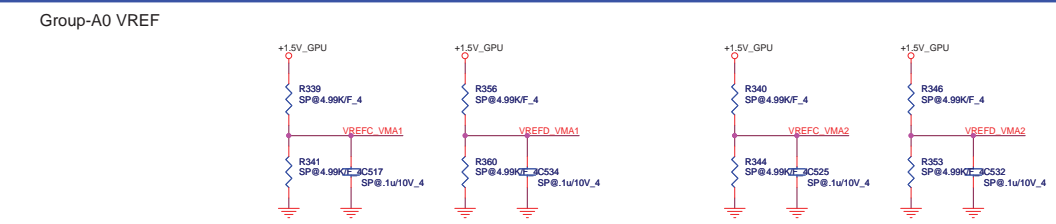
TOP Left

BOT Left

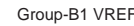


BOT Right

TOP Right

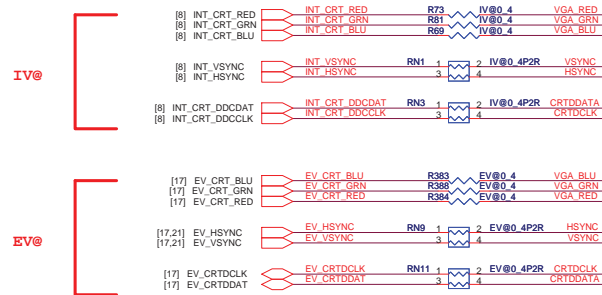


Park, M92M Use Channel B Memory Interface Only

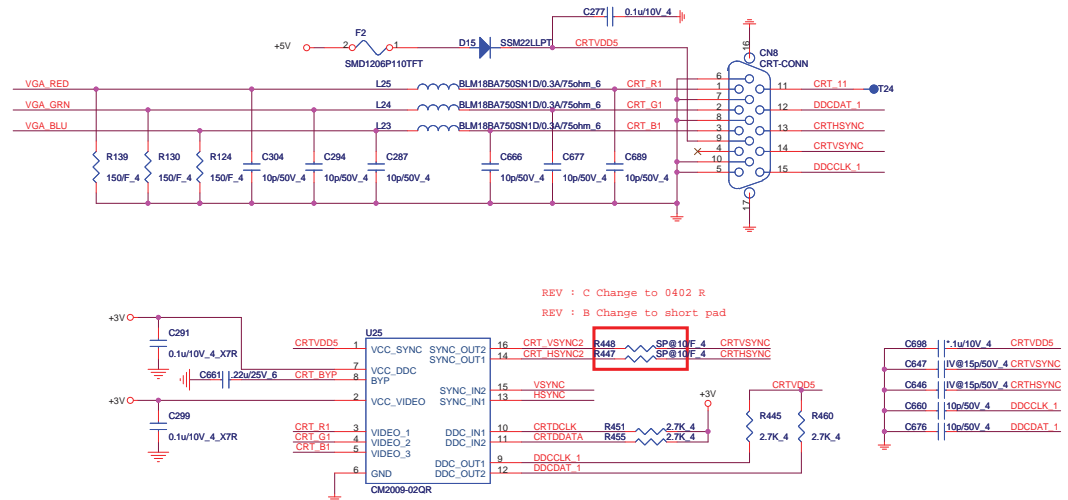


CRT Switch

0_ohm Resistor place close to Joint-Point

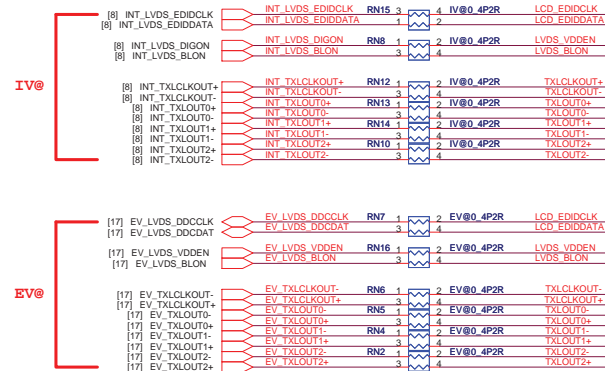


CRT

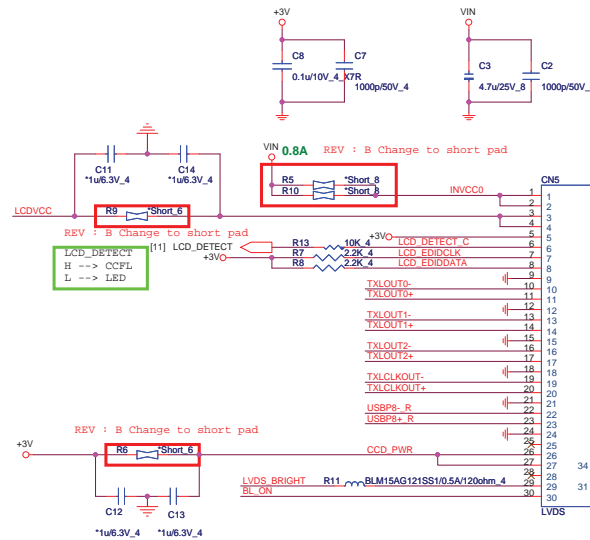


LVDS

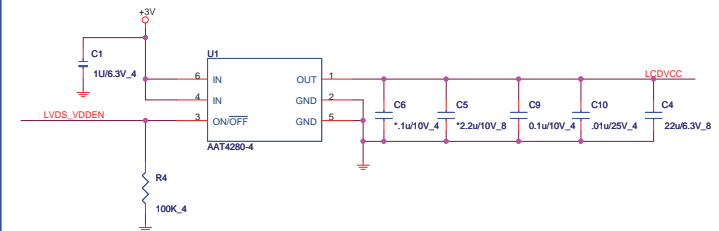
0_ohm Resistor place close to Joint-Point



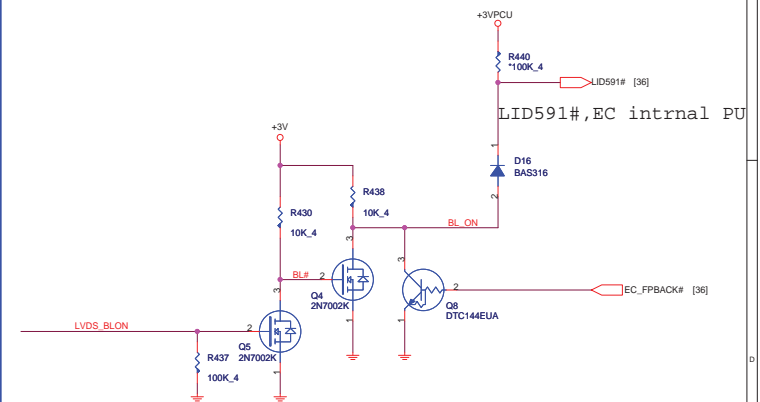
LVDS



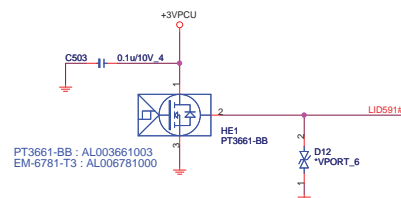
LCD Power



Backlight Control

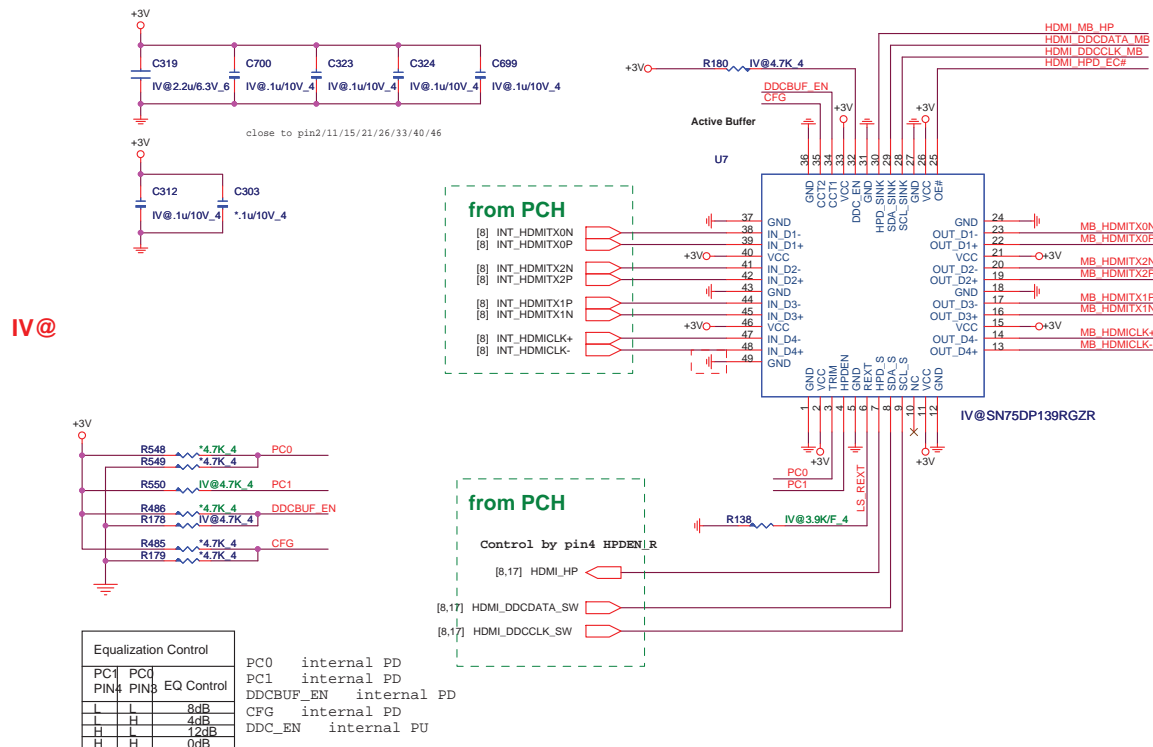


Lid Switch (Hall sensor)



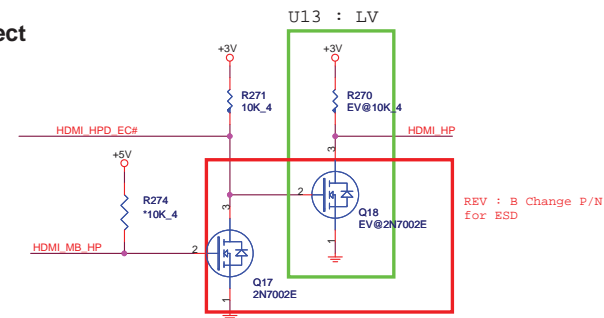
CCD +3V-current budget 0.2A

HDMI LEVEL SHIFTER



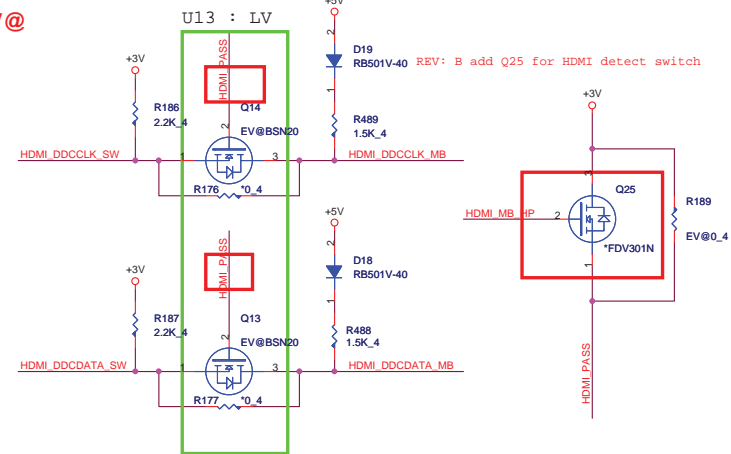
HDMI-detect

EV@



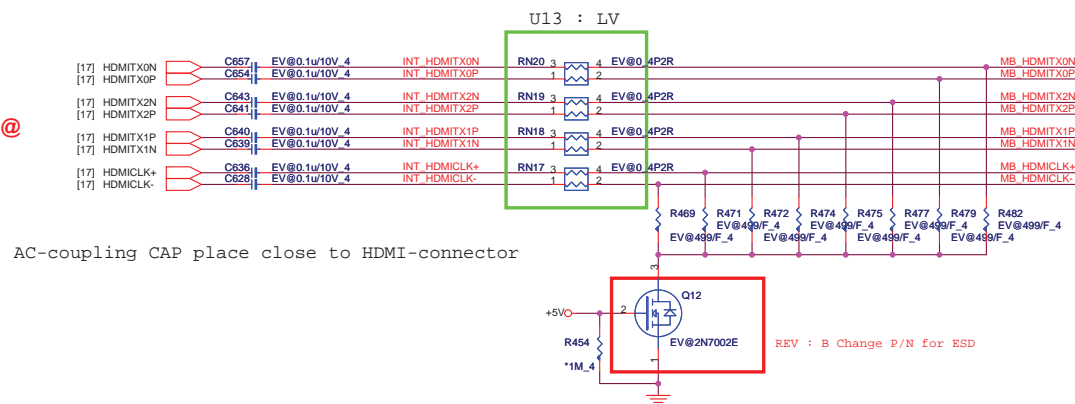
I2C

EV@

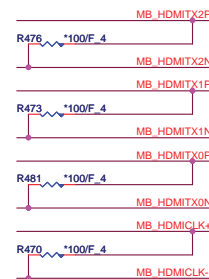


Switchable Graphic HDMI source

EV@

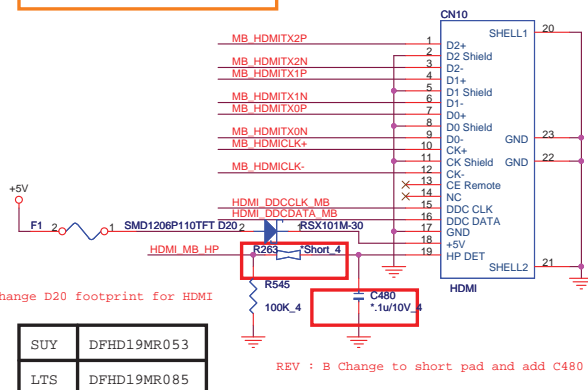


EMI

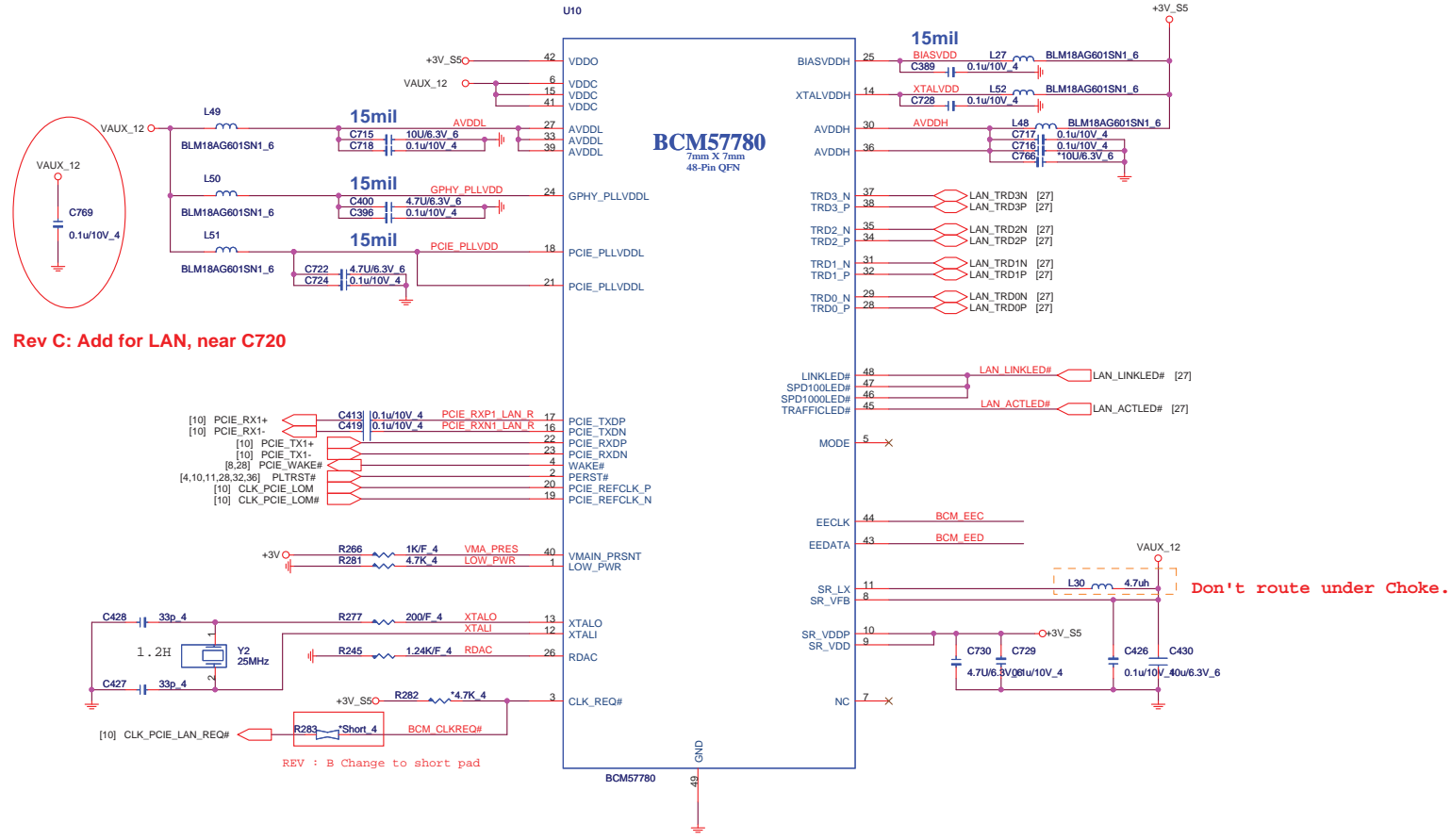


HDMI connector

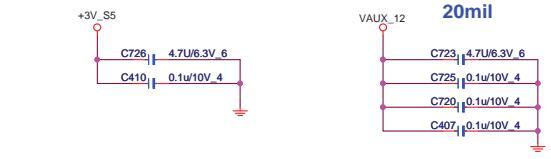
REV : C Location :D20 Change Footprint & P/N



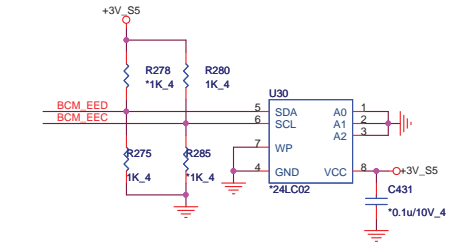
Giga-LAN BCM57780



LAN POWER



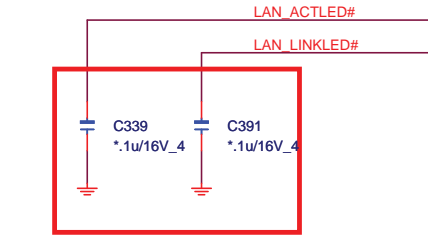
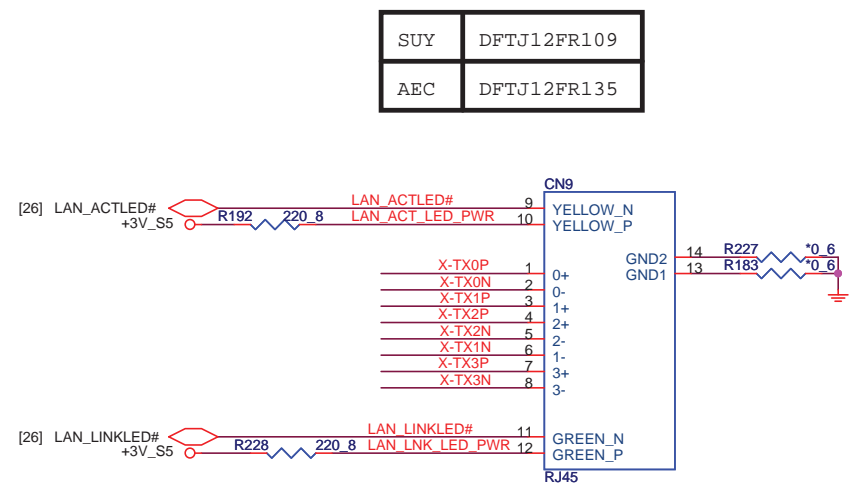
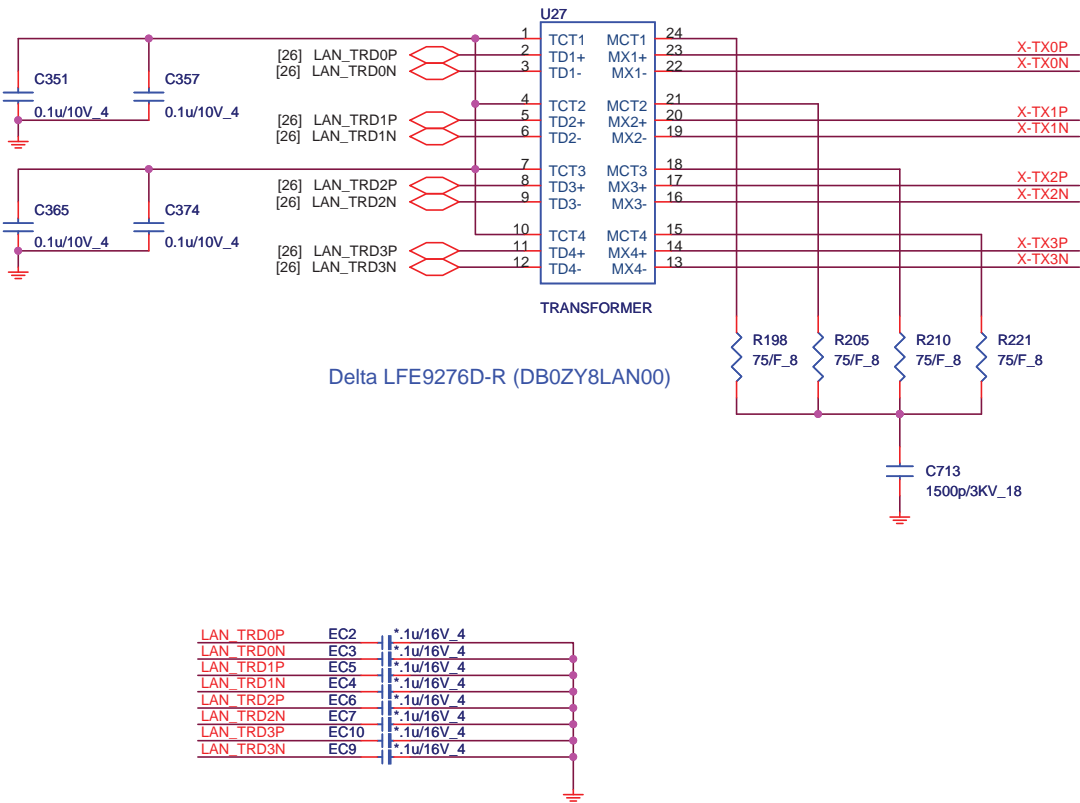
EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

TRANSFORMER



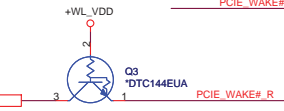
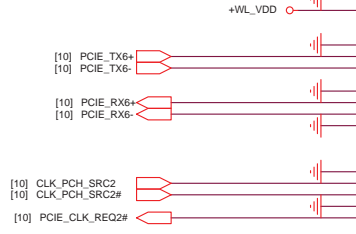
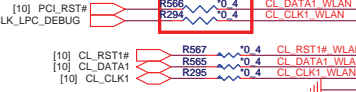
REV : B Change to 0402 for ESD

MINI-CARD WLAN(MPC)

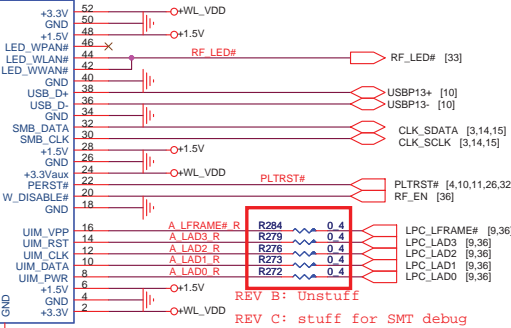
+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

REV : B Unstuff

Debug

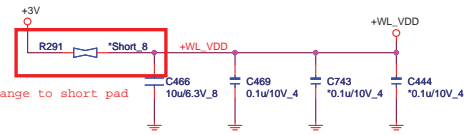


H=7.0mm
LTS AAA-PCI-046-K01

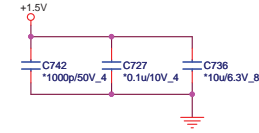


REV B: Unstuff
REV C: stuff for SMT debug

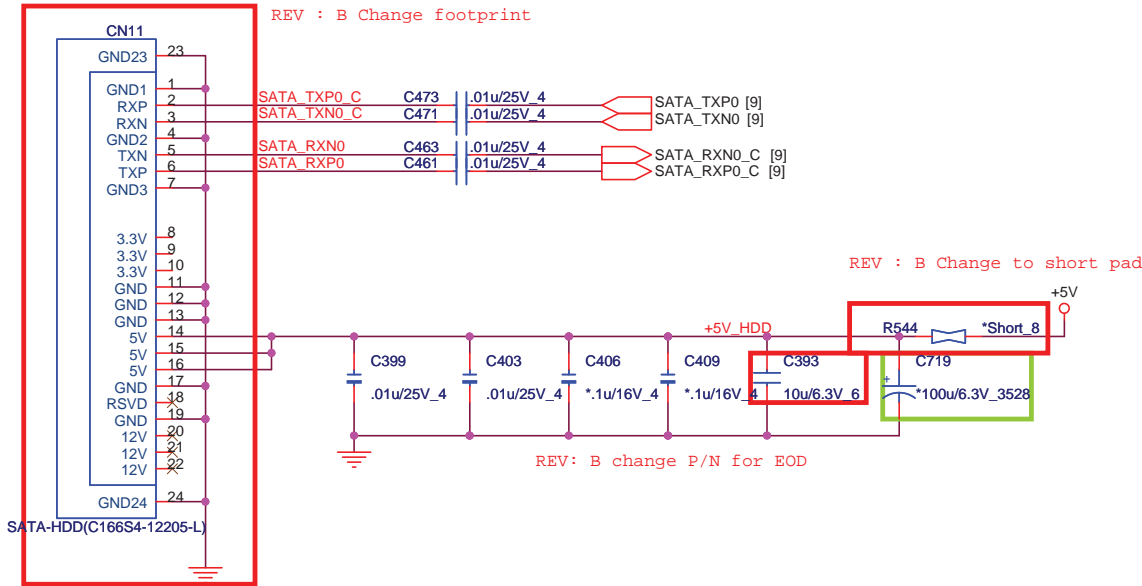
Debug



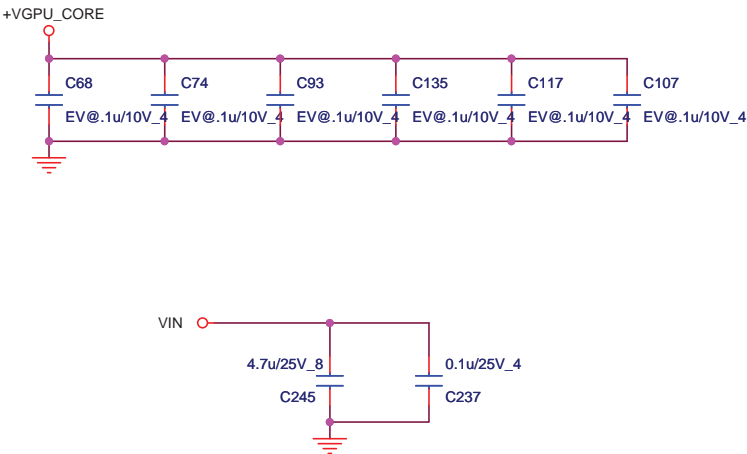
REV : B Change to short pad



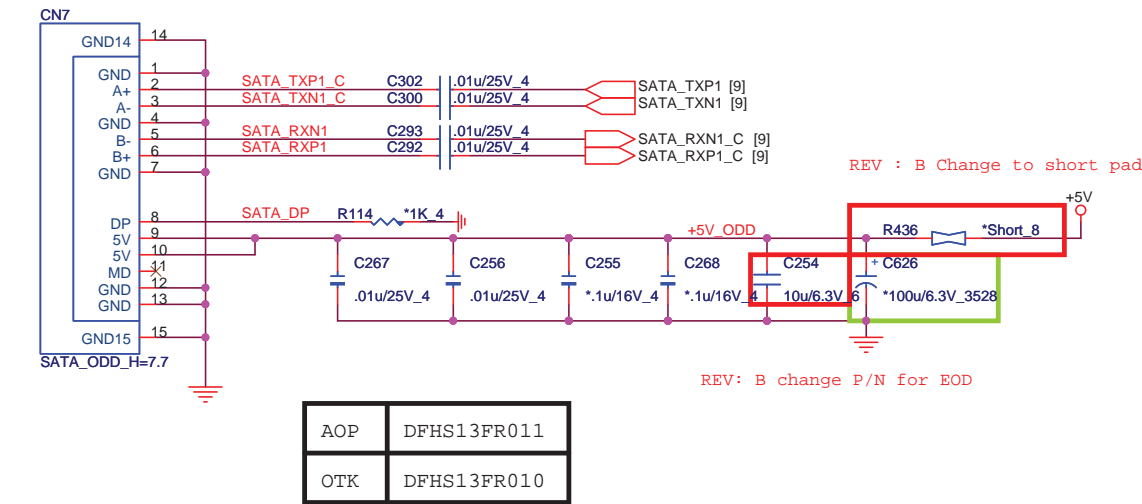
MAIN SATA HDD



EE RETURN-PATH CAPACITORS




ODD (SATA)



SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

AOP	DFHS13FR011
OTK	DFHS13FR010

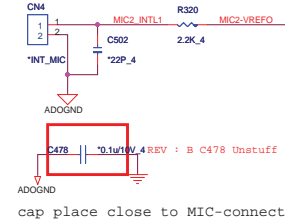
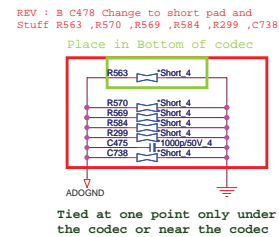
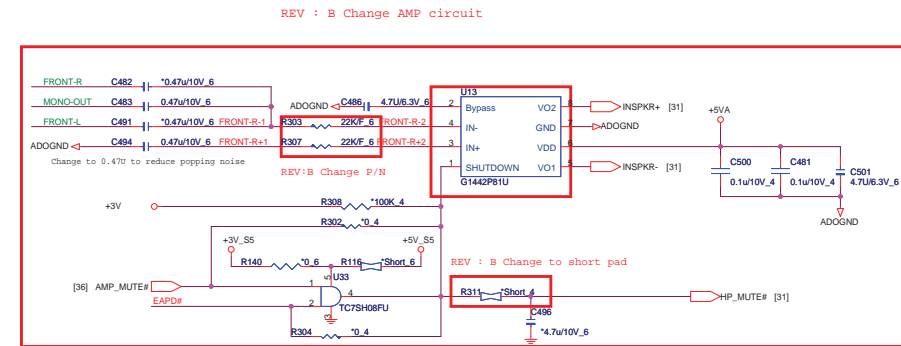



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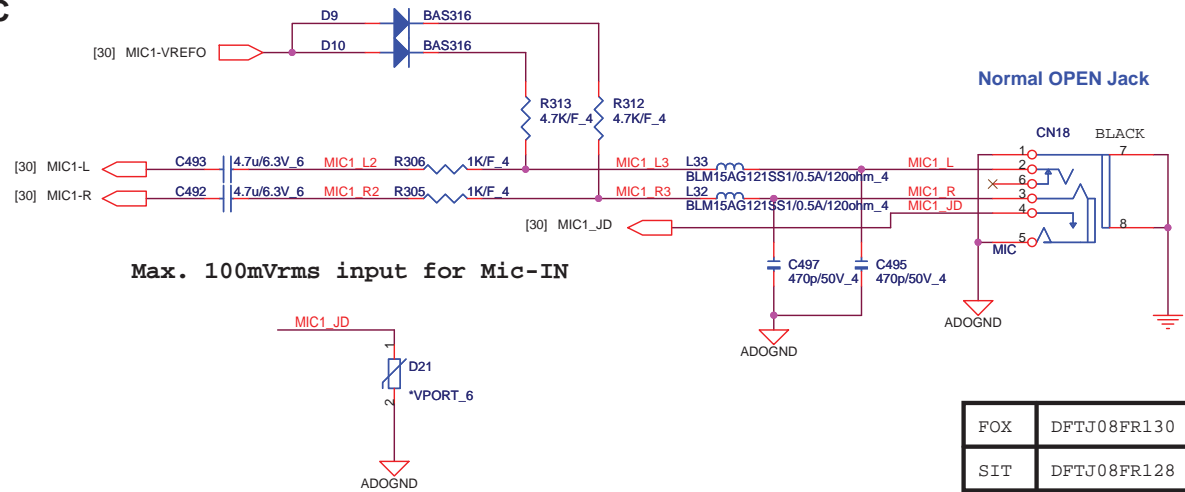
Size	Document Number	Rev
	SATA-HDD/ODD/RETURN-PATH	1C
Date:	Wednesday, July 21, 2010	Sheet 29 of 46

MUTE(AMP)

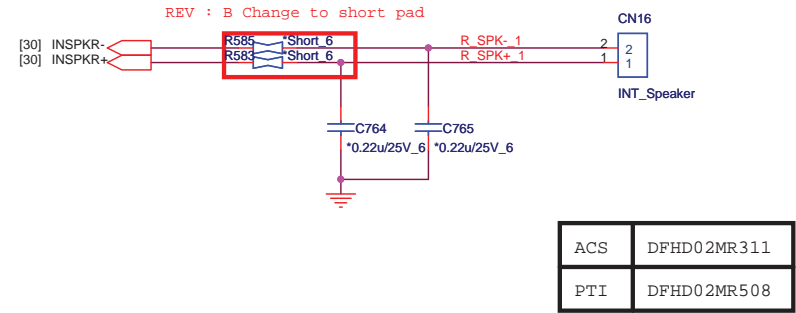


 <div> Quanta Computer Inc. PROJECT : ZRD </div>		Rev 1C
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REALTEK ALC663&888/MDC		
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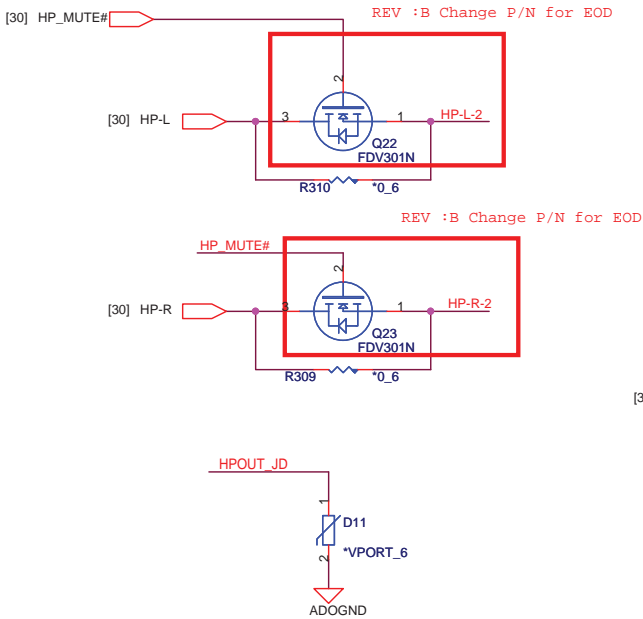
MIC



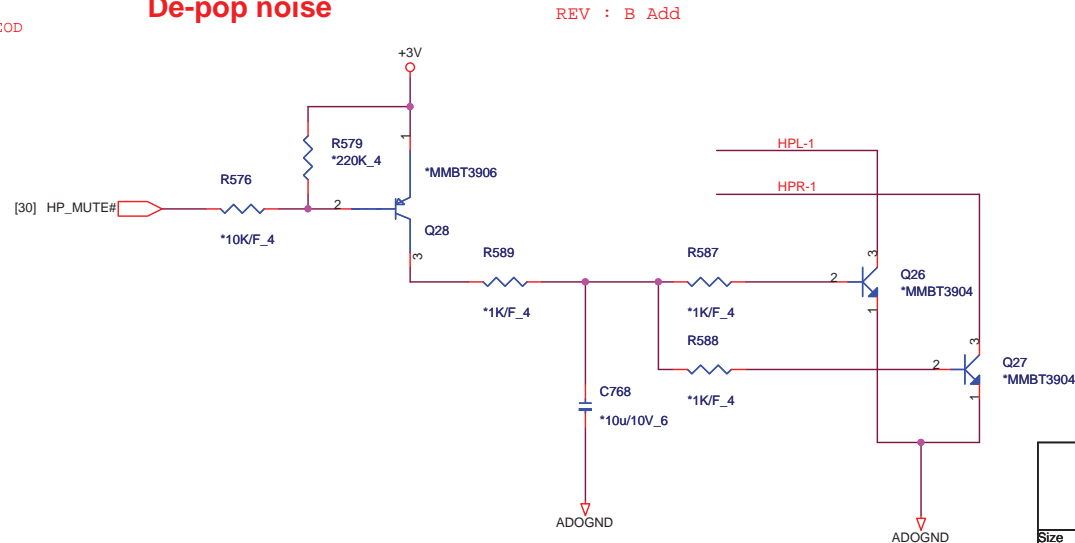
Internal Speaker



HP/SPDIF

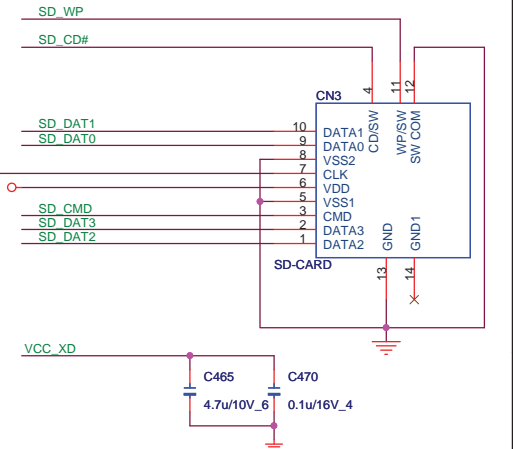
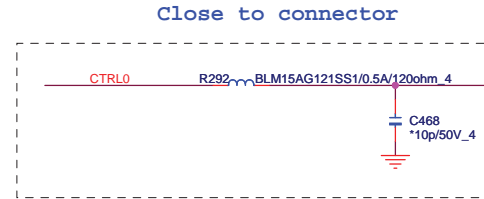
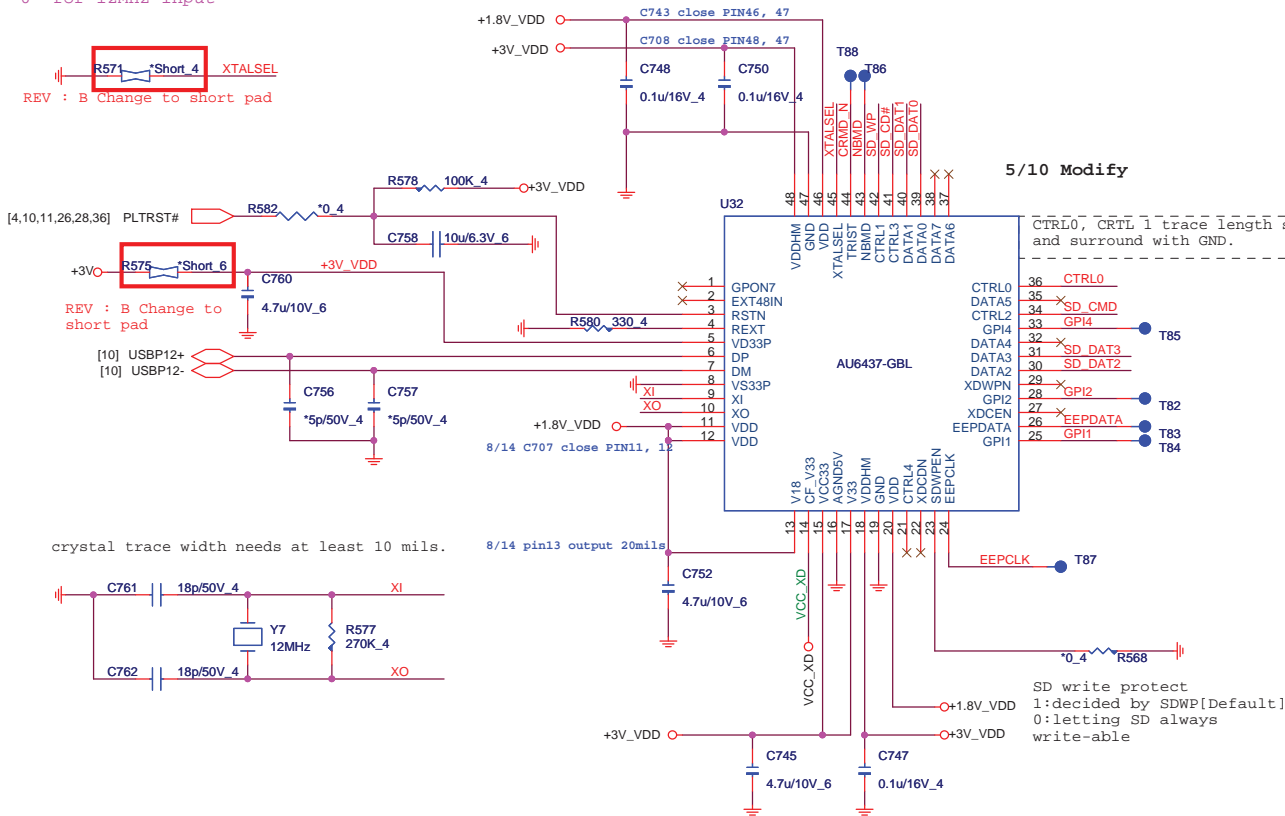
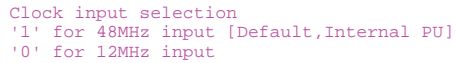


De-pop noise




CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

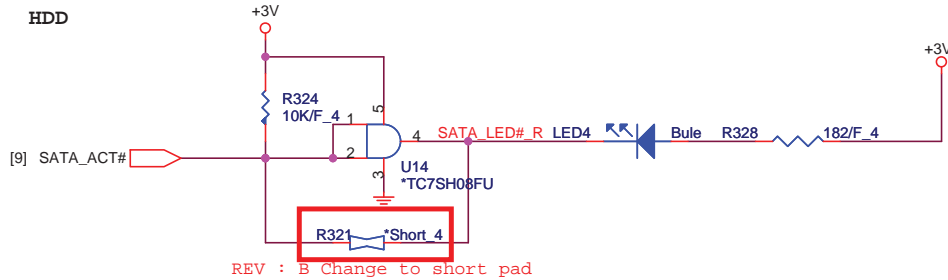


PNT	DFHS11FR011
PLA	DFHS11FR033

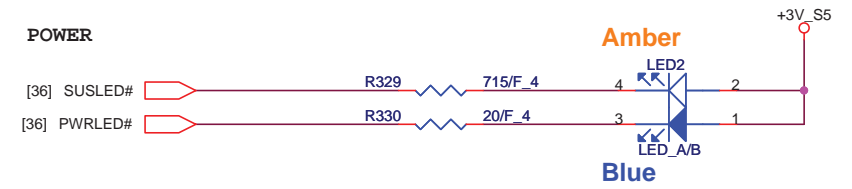
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

	PROJECT : ZQ5 Quanta Computer Inc.			
	Size	Document Number		Rev
		AU6433 CardReader		1C
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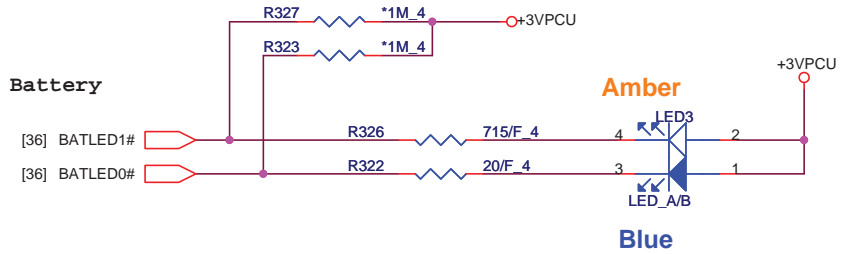
LED



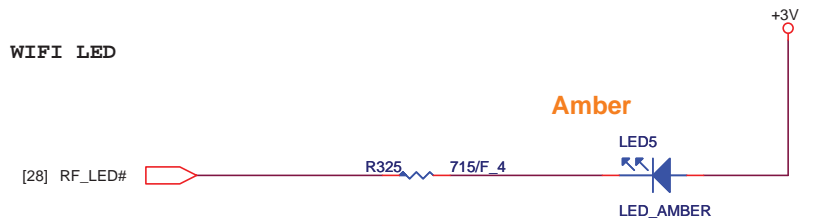
POWER



Battery



WIFI LED



Quanta Computer Inc.

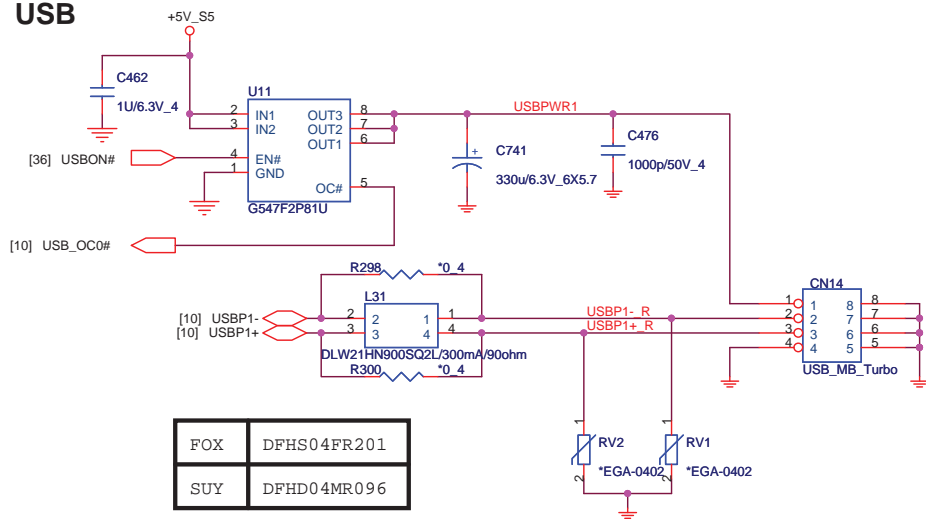
PROJECT : ZRD

Size	Document Number	Rev 1C
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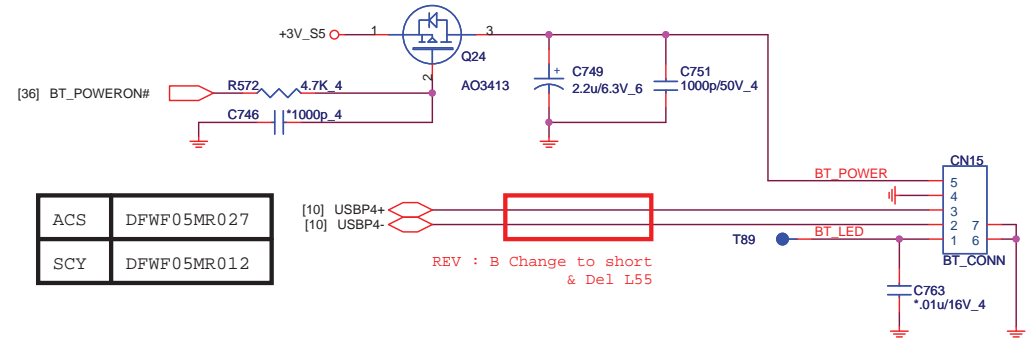
POWER/MMB/LAUNCH/LED

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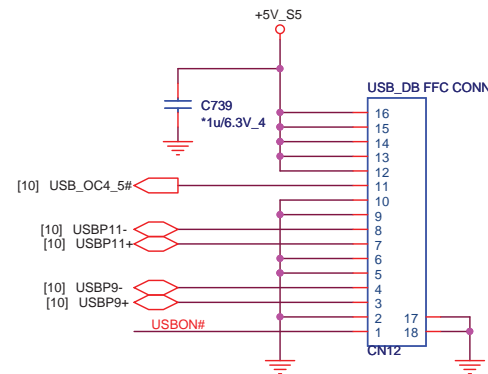
USB



BLUETOOTH CONNECTOR



USB/B



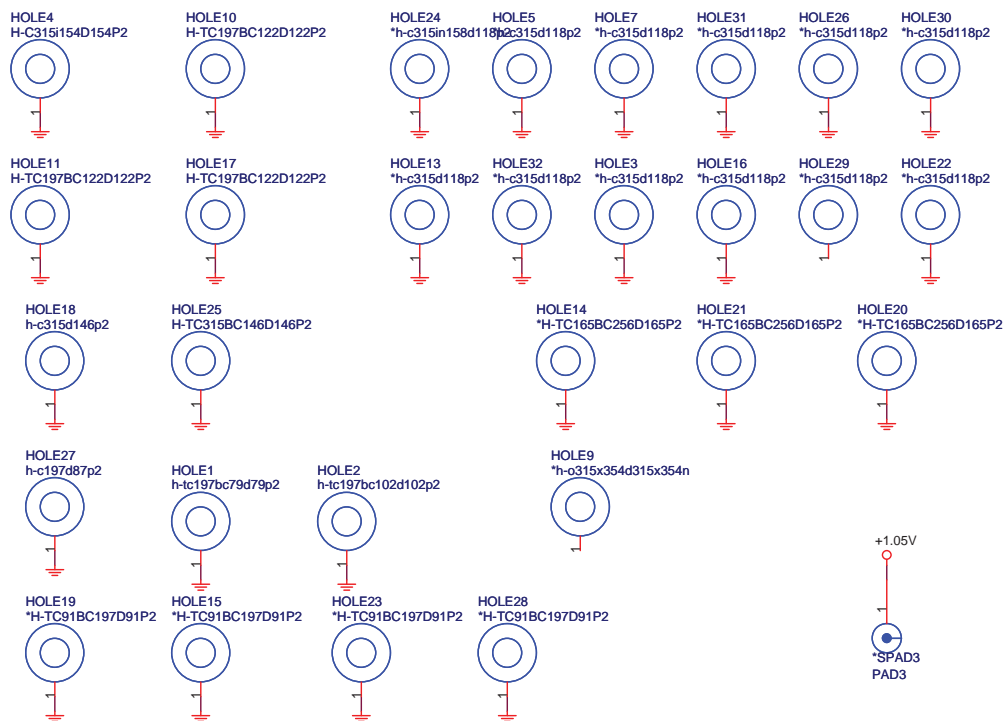
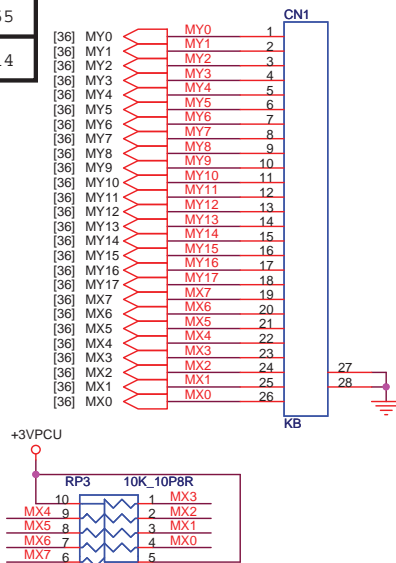
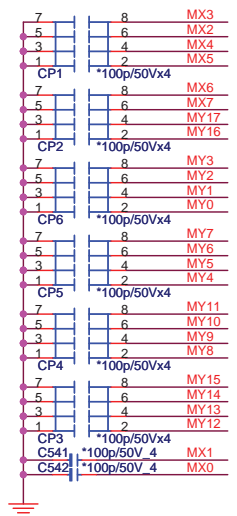
Quanta Computer Inc.

PROJECT : ZRD

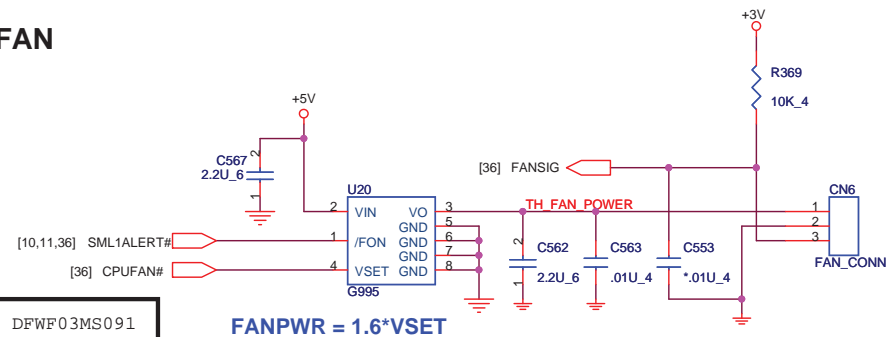
Size	Document Number	Rev
	USB/ BT	1C

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PTI	DFFC26FR155
ACS	DFFC26FR014

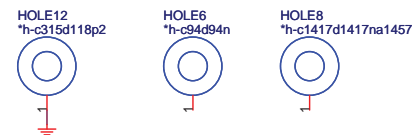
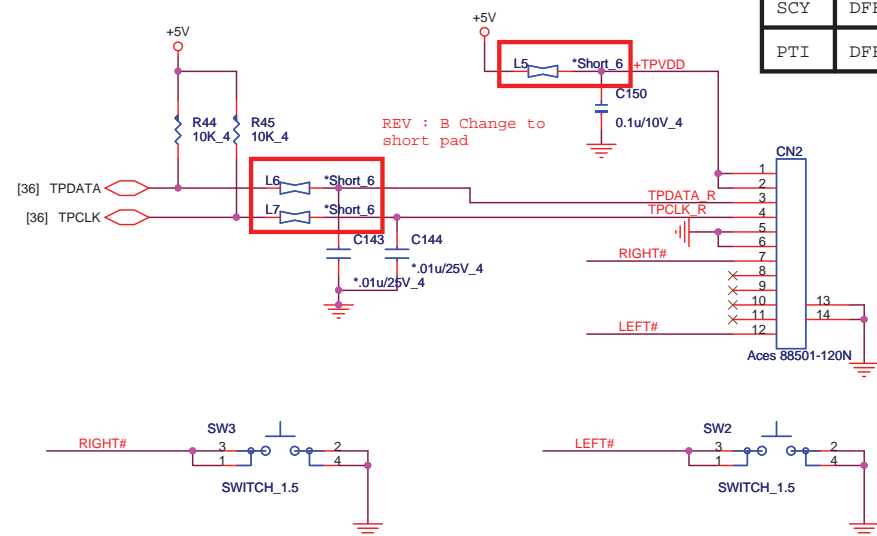



ACS	DFWF03MS091
SCY	DFWF03MS000



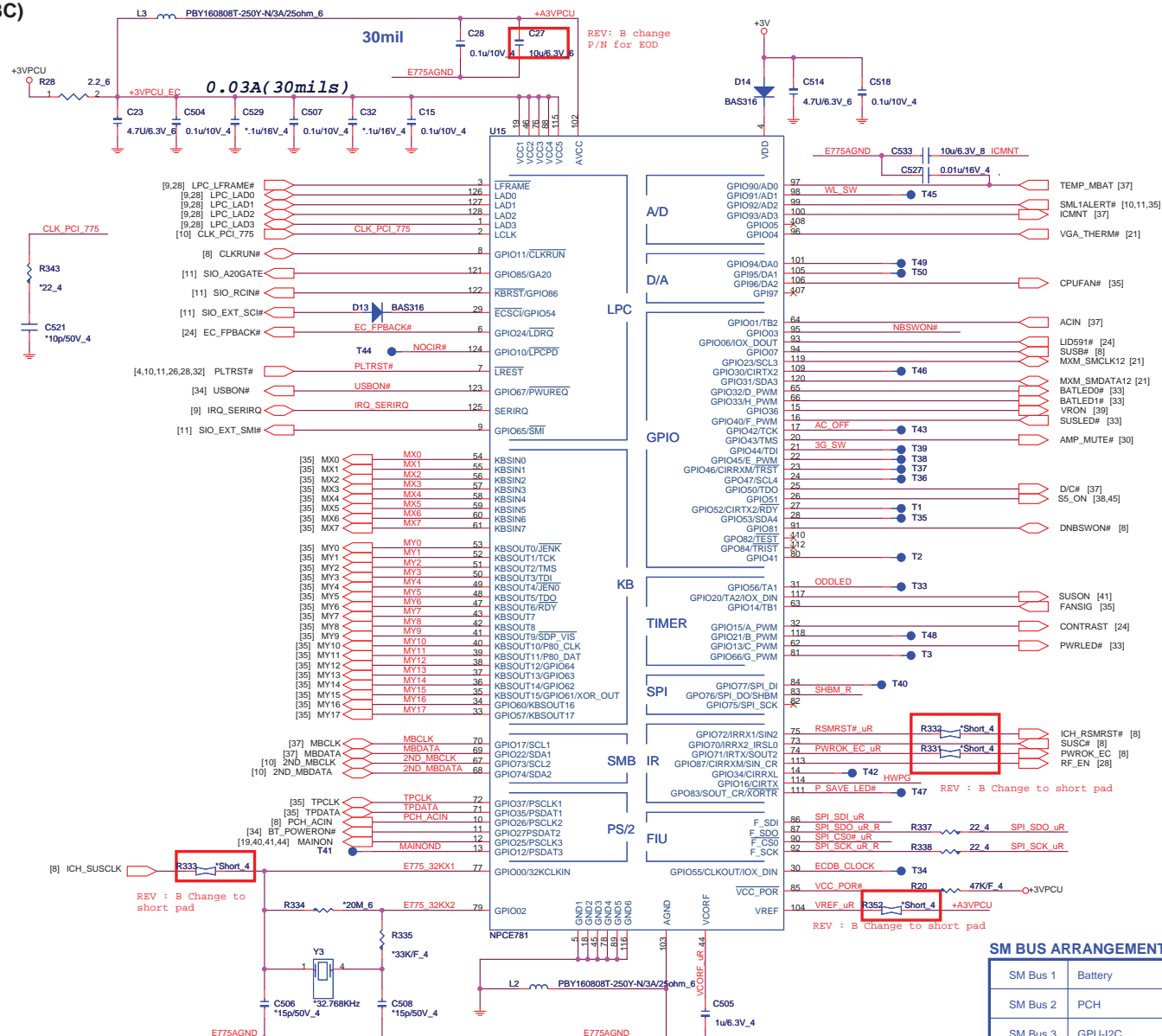
TOUCHPAD & Switch CONN.

ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234



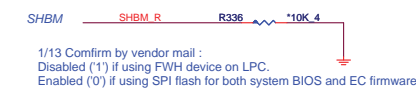
 Quanta Computer Inc. PROJECT : ZRD	
Size	Document Number
KB/FAN/TP+FP	
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EC(KBC)

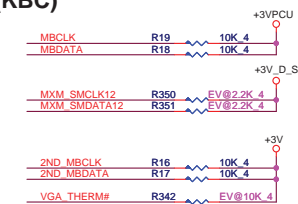


I/O ADDRESS SETTING(KBC)

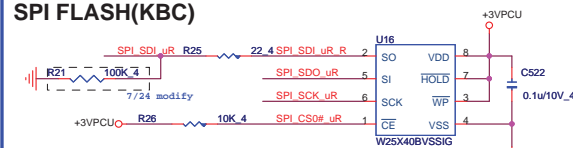
SHBM=0: Enable shared memory with host BIOS



SM BUS PU(KBC)

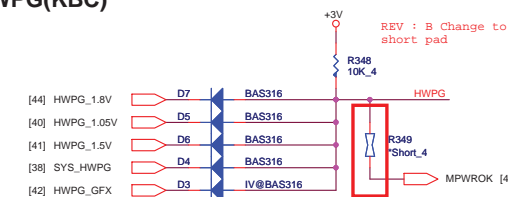


SPI FLASH(KBC)

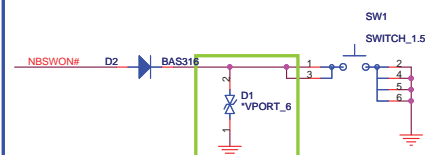


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG(KBC)



POWER-ON Switch(KBC)



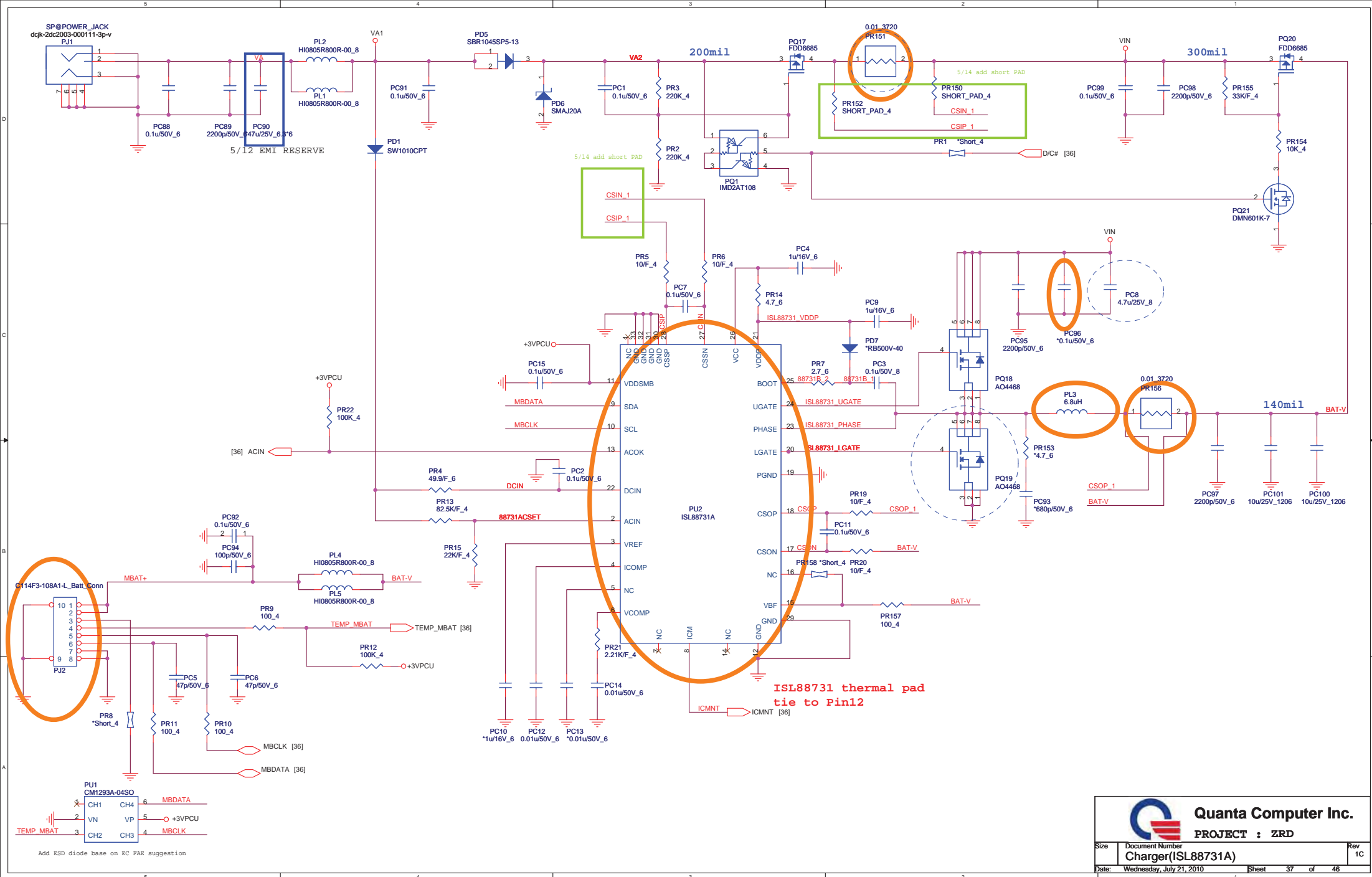
5/13 change the location

INTERNAL KEYBOARD STRIP SET(KBC)

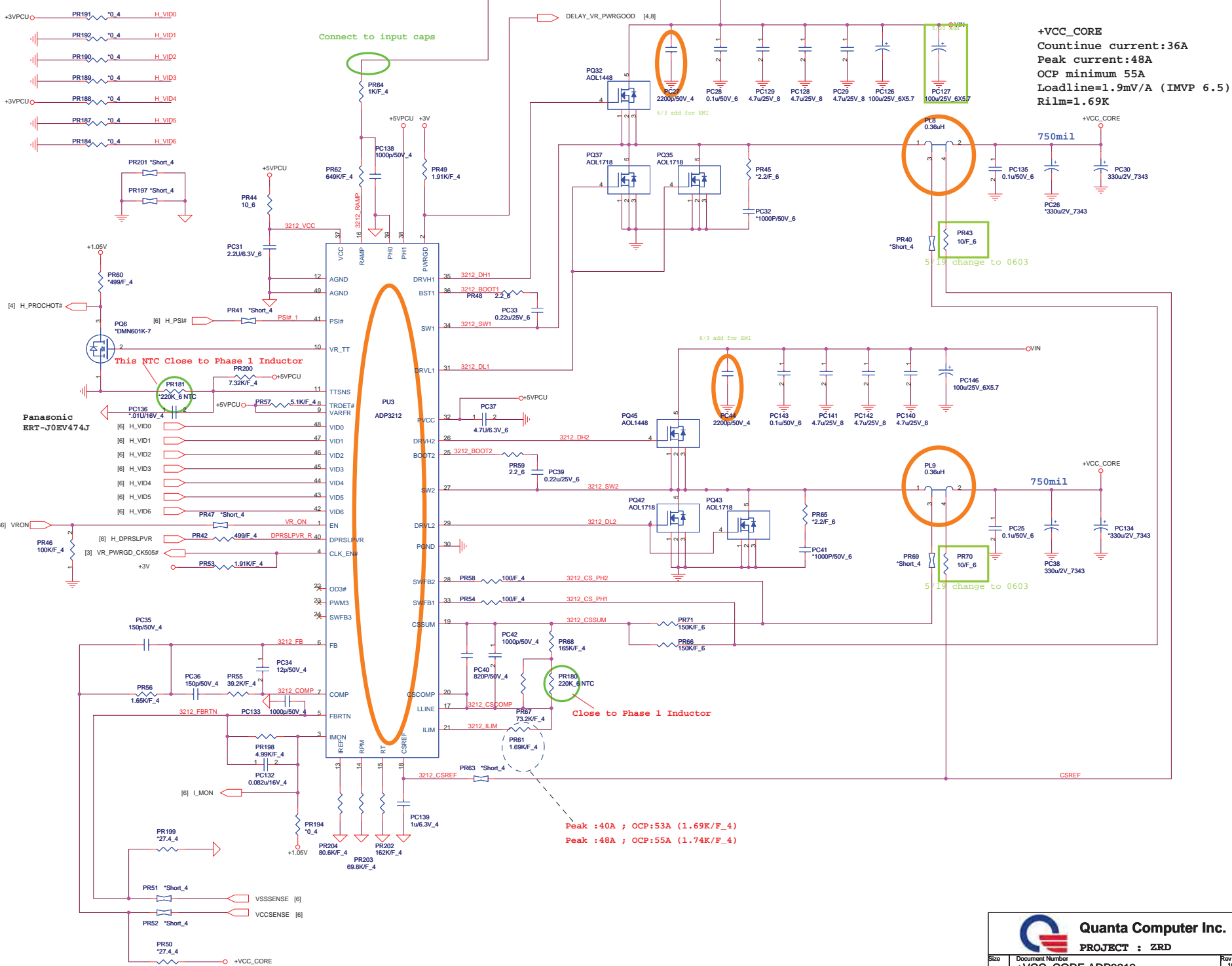
**Quanta Computer Inc.**

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	WPCE781 & FLASH	
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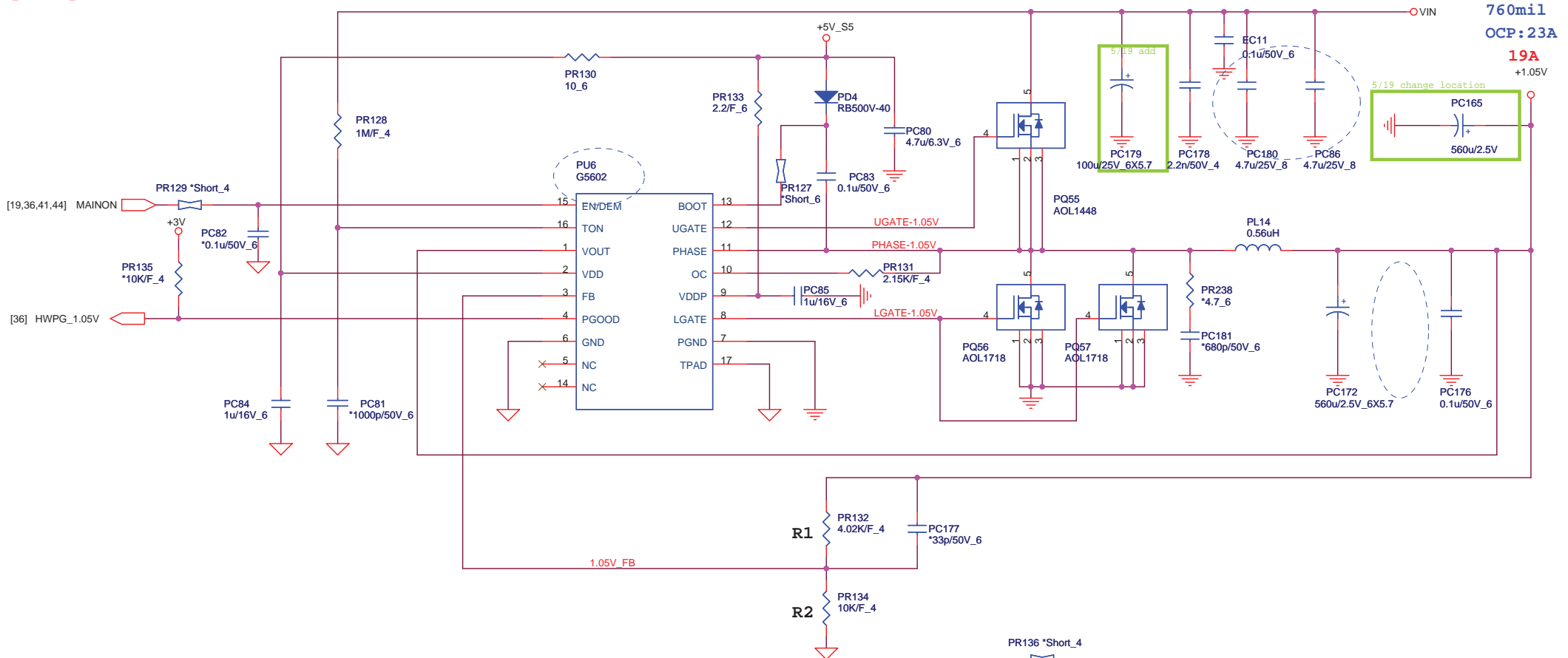
VID 1.2875V



Quanta Computer Inc.
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	+VCC_CORE ADP3212	1C
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[PWM]



$$T_{ON}=3.85p \cdot R_{TON} \cdot V_{out} / (V_{in}-0.5)$$

$$\text{Frequency} = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON}=3.85p*1M*1/(V_{in}-0.5)$$

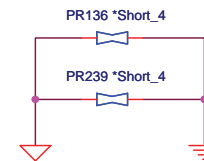
$$\text{Frequency} = 1 / (0.0036767) = 272\text{K}$$

AO1718 Rdson=3~4.3mOhm

```
L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A
```

$$R_{ILIM} = 2.15\text{mohm} * 23 - 3.256 / 20\text{uA} = 2.122\text{Kohm}$$

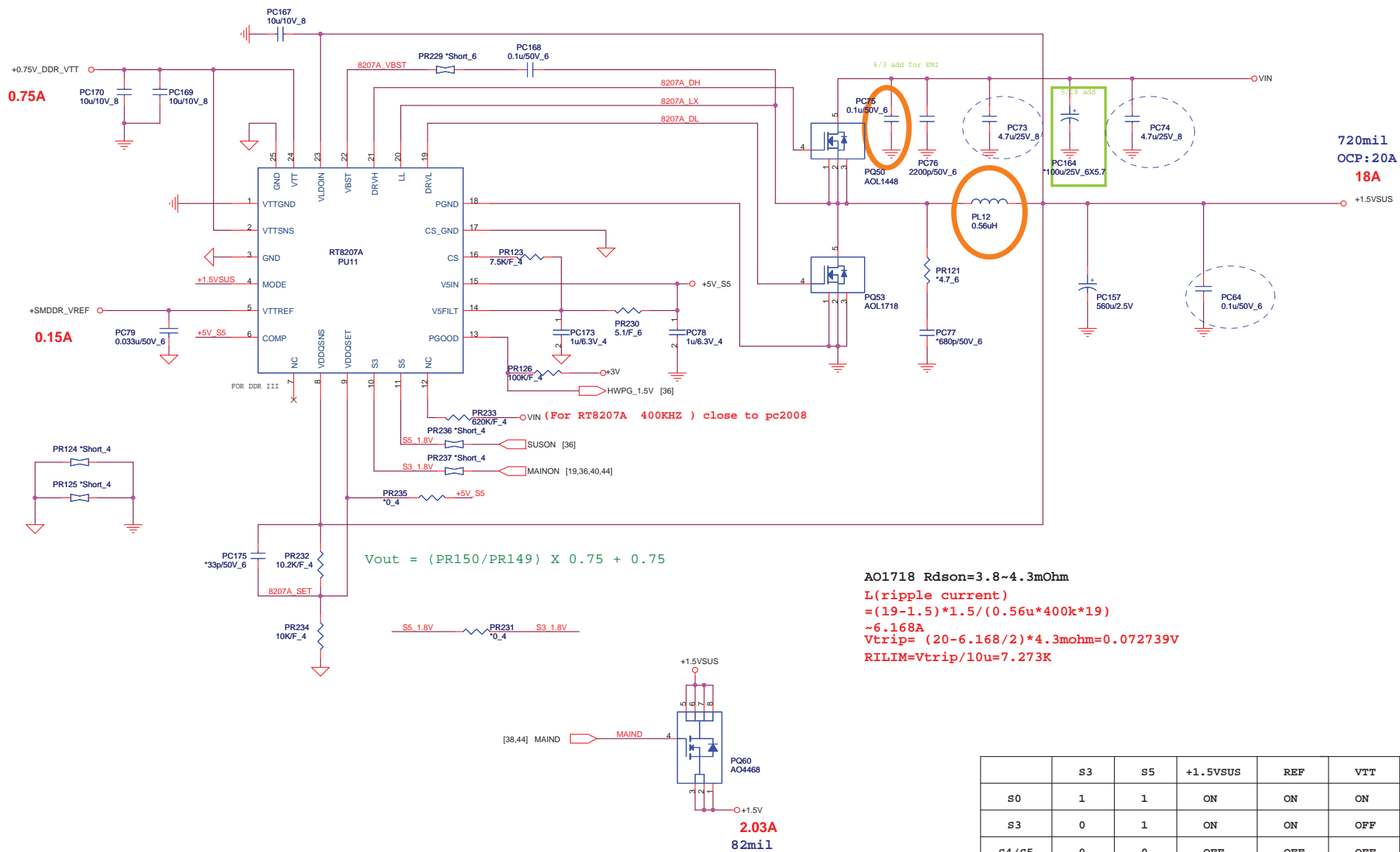
I (choke)peak=29.512A



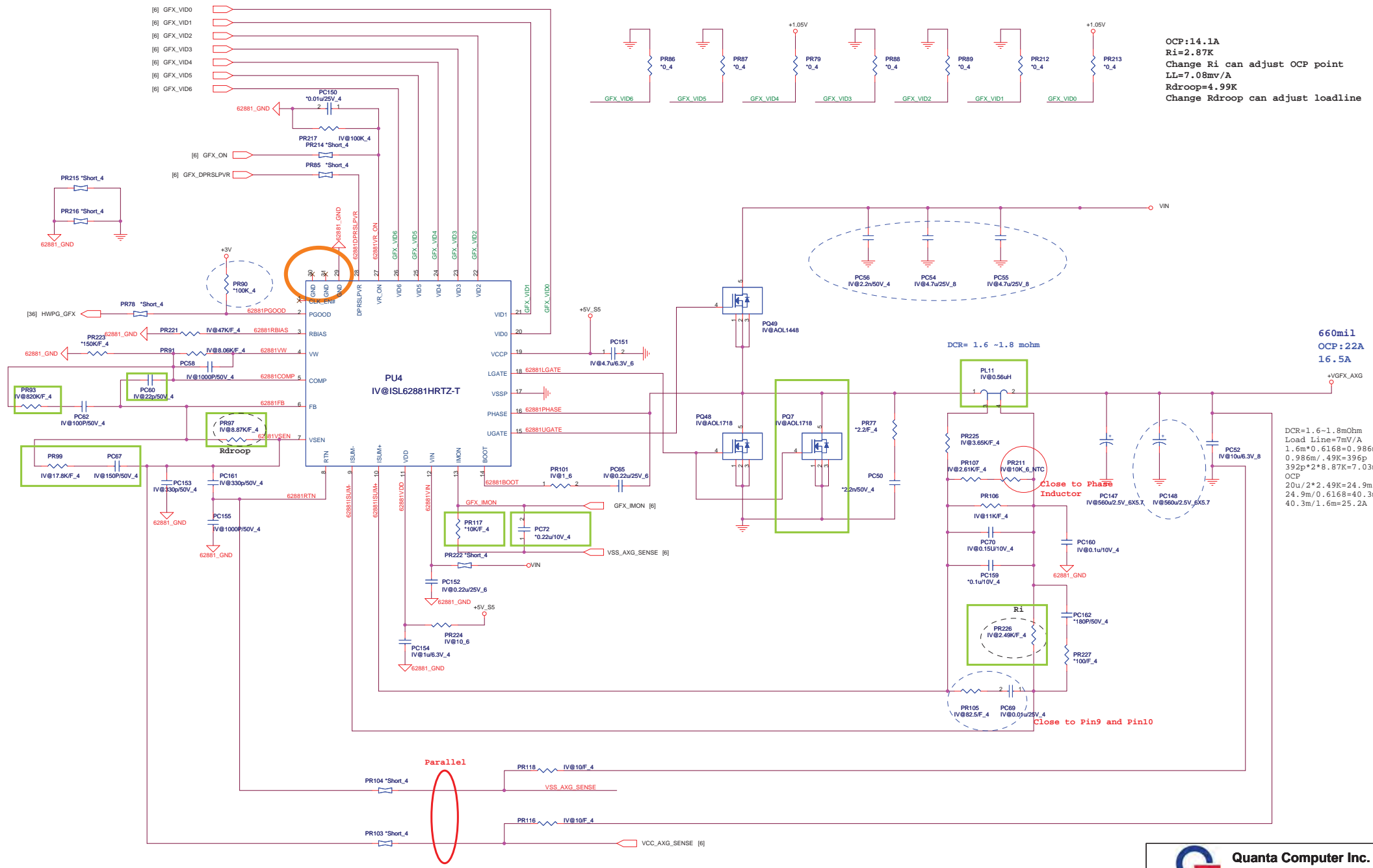
Quanta Computer Inc.
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[PWM]



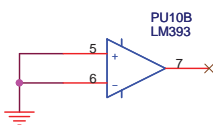
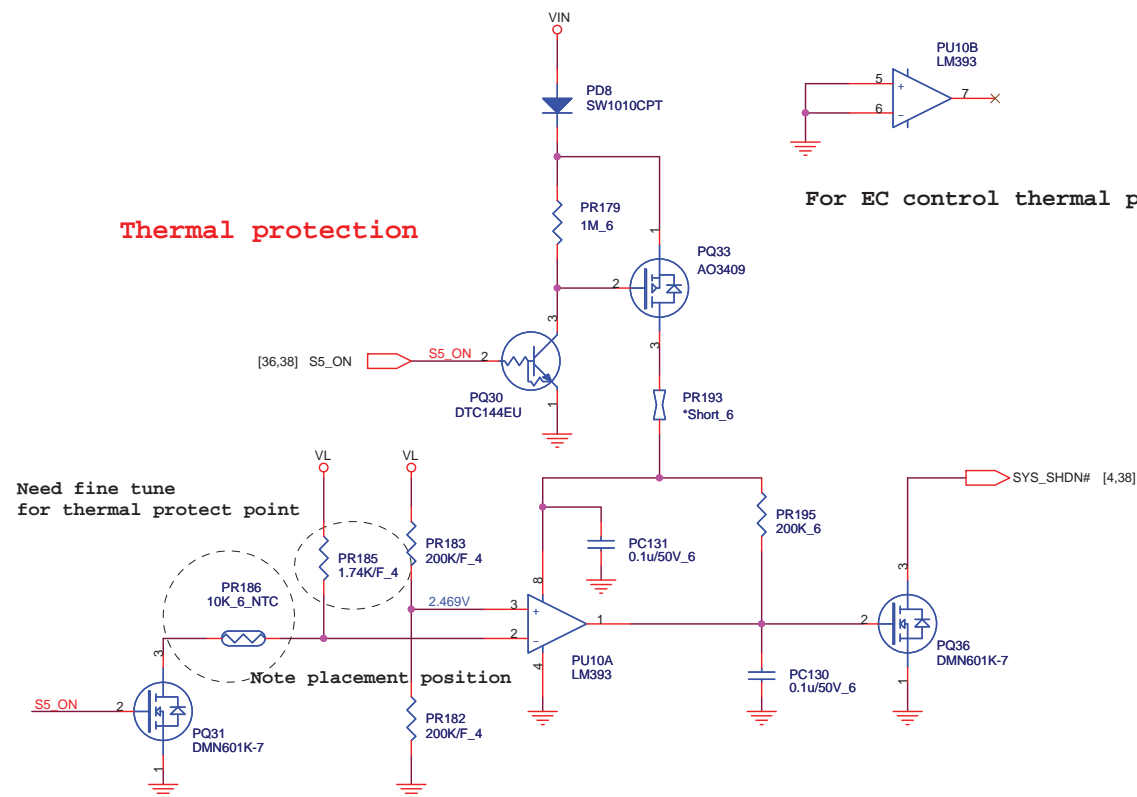
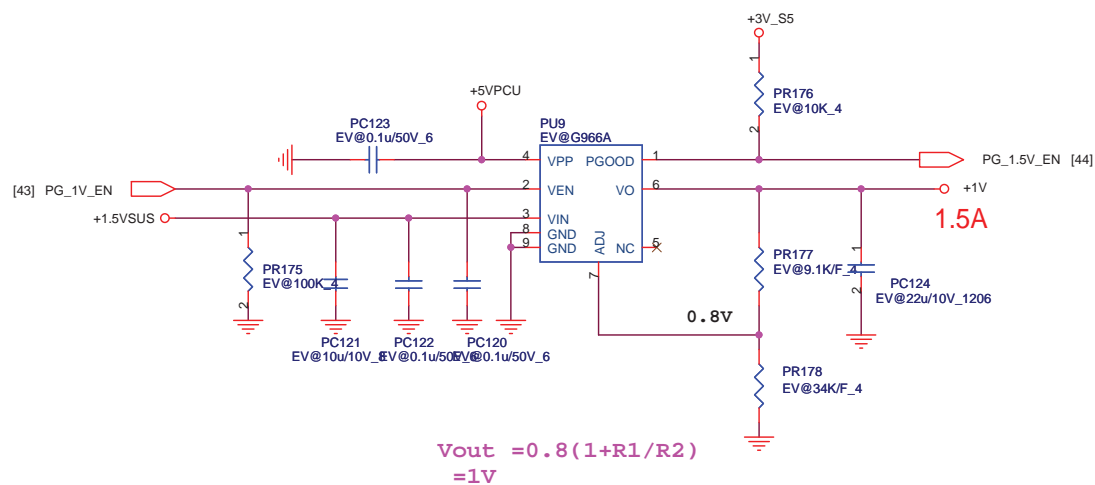
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



OCP:14.1A
Ri=2.87K
Change Ri can adjust OCP point
LL=7.08mv/A
Rdroop=4.99K
Change Rdroop can adjust loadline

660mil
OCP:22A
16.5A

DCR=1.6~1.8mohm
Load Line=7mV/A
1.6m*0.6168=0.986m
0.986m/.49K=396p
392p*2*8.87K=7.03m
OCP
20u/2*2.49K=24.9m
24.9m/0.6168=40.3m
40.3m/1.6m=25.2A



For EC control thermal protection (output 3.3V)



Quanta Computer Inc.
PROJECT : ZRD

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		1C
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Model	REV	CHANGE LIST	MODEL	ZRD	
ZRD MB				FROM	To
	1A	FIRST RELEASED		X	1A
				X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
2A	Page 3 : Unstuff L54 & stuff R586 & change U31 P/N for 3V CLK gen and Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL Page 4 : Q16 Change P/N for EOD part & short R116 (Del.) for 0 ohm Page 8 : Short R244 (Del.) for 0 ohm Page 10 : Short R243 (Del.) for 0 ohm Page 12 : Short R189 , R190 & R534 (Del.) for 0 ohm & C655 change P/N for EOD part Page 14 : Del. R288 & R247 for R3 solution & stuff R269 , R229 , R223 & R326 for R1 solution ,stuff C372 for +1.5VSUS leakage Page 15 :stuff C459 for +1.5VSUS leakage Page 25 : Q12 , Q17 & Q18 change P/N for ESD , CN10 Change P/N ,Q14.2 & Q13.2 Change from +5V to +3V Page 27 : C339 & C391 of footprint change from 0805 to 0402 for ESD Page 28 : Unstuff R516 , R294 , R284 , R279 , R576 , R273 , R272 for disable debug card function Page 29 : C393 & C254 Change P/N for EOD , CN11 Change footprint for ME design request. Page 30 : U13 Change AMP circuit Page 31 : C22 & C23 change P/N for MOD part. Page 34 : Del. L55 , CN12 Change P/N Page 36 : C27 Change P/N for EOD part Page A11 : Change to short pad : Location : R458 ,R452 ,R537 ,R533 ,R144 ,R155 ,R191 ,R140 ,R201 ,R224 ,R461 ,R136 ,R197 ,R206 ,R219 ,R212 ,R166 ,R174 ,R188 ,R202 ,R209 ,R184 ,R168 ,R185 ,R448 ,R447 ,R5 ,R10 ,R9 ,R6 ,R263 ,R288 ,R544 ,R436 ,R563 ,R570 ,R569 ,R584 ,R299 ,C738 ,R311 ,R585 ,R583 ,R571 ,R582 ,R575 ,R576 ,R579 ,R333 ,R352 ,R331 ,R332 & R349		1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
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